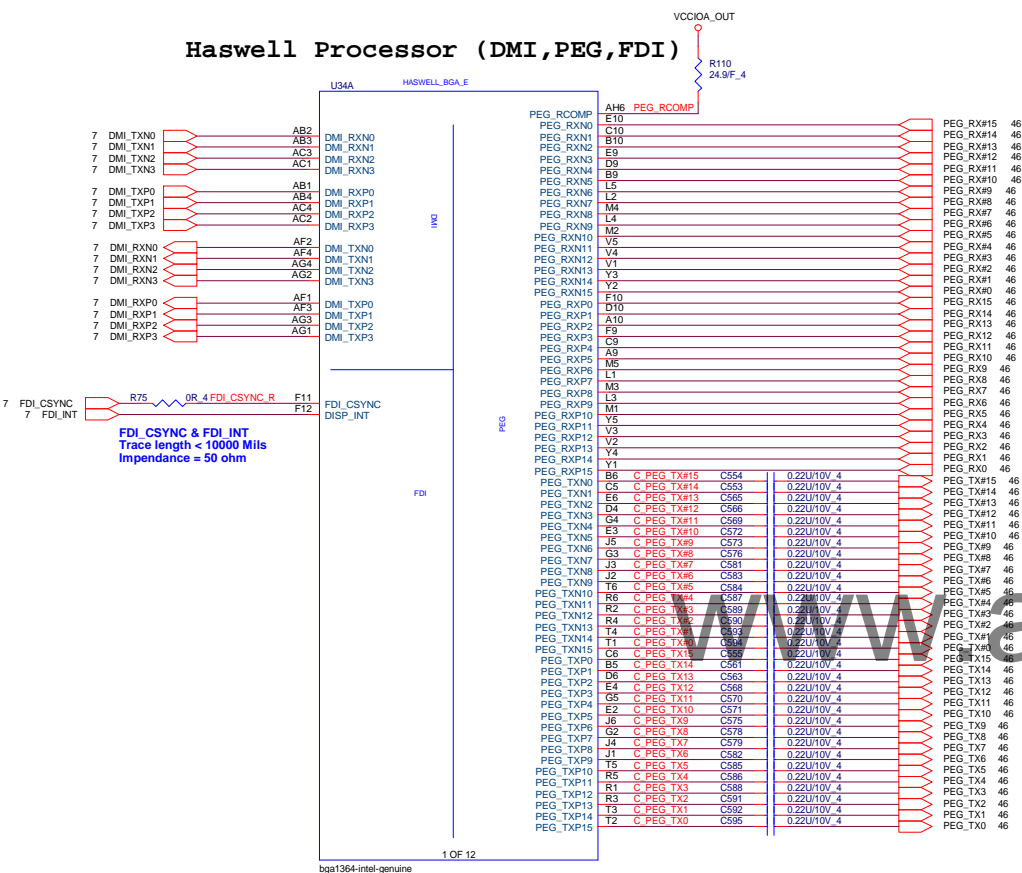


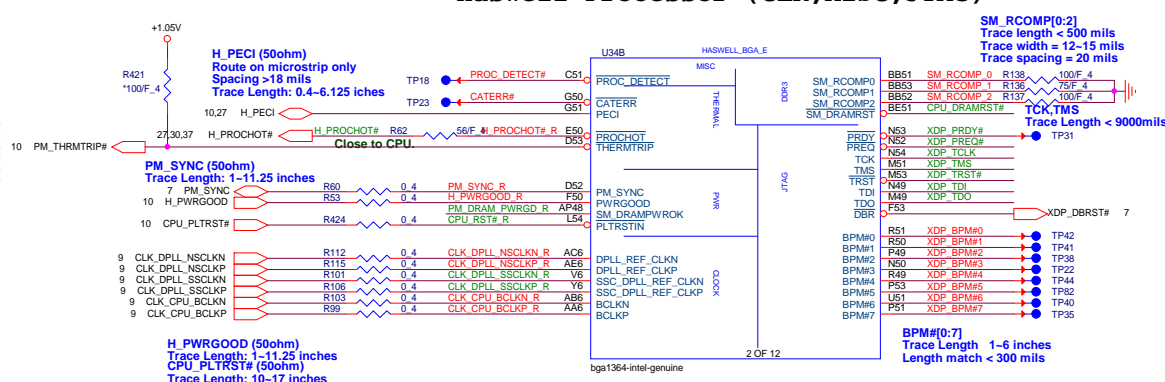
I7-4860 CPU--AJ0QDY0UT00

PEG_RCOMP
Trace length < 400 MILS
Trace width = 12 MILS
Trace spacing = 15 MILS

Haswell Processor (DMI,PEG,FDI)



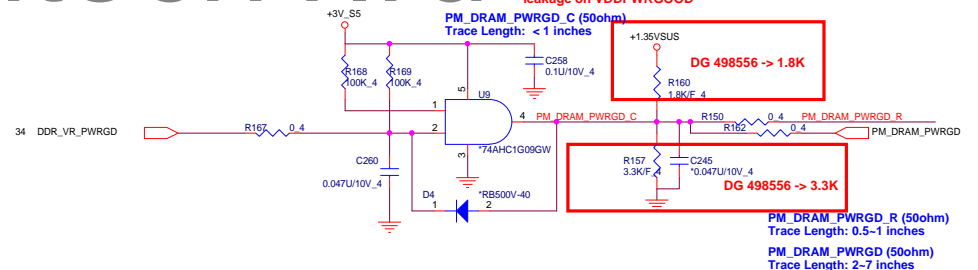
Haswell Processor (CLK,MISC,JTAG)



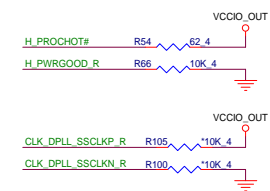
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SM_DRAMPWROK Processor Input.

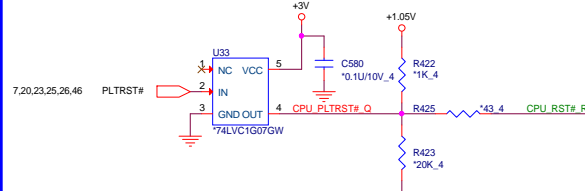
To change the resistor values in the DRAMPWROK logic to reduce the leakage on VDDPWRGOOD



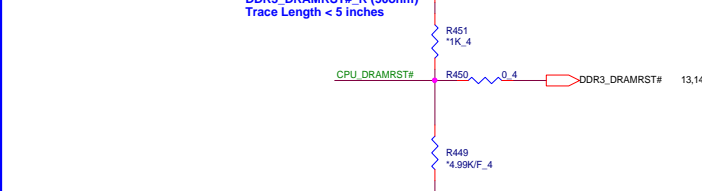
PU/PD of CPU



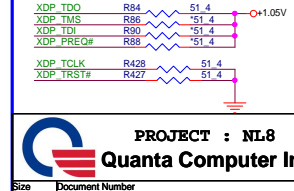
Reserved For buffer reset of PLTRST#



SM_DRAMRST# Topology



XDP PU/PD



Haswell Processor (DDI,eDP,FDI)

2,5 VCCIOA_OUT
2,5,37 VCCIO_OUT

04

HDMI

17 HDMI_TX2-
17 HDMI_TX2+
17 HDMI_TX1-
17 HDMI_TX1+
17 HDMI_TX0-
17 HDMI_TX0+
17 HDMI_CLK-
17 HDMI_CLK+

C25 DDIB_TXN0
D25 DDIB_TXP0
A25 DDIB_TXN1
B25 DDIB_TXP1
C24 DDIB_TXN2
D24 DDIB_TXP2
A24 DDIB_TXN3
B24 DDIB_TXP3

C21 DDIC_TXN0
D21 DDIC_TXP0
A21 DDIC_TXN1
B21 DDIC_TXP1
C20 DDIC_TXN2
D20 DDIC_TXP2
A20 DDIC_TXN3
B20 DDIC_TXP3

C16 DDID_TXN2
D16 DDID_TXP2
A16 DDID_TXN3
B16 DDID_TXP3

C17 DDID_TXN0
D17 DDID_TXP0
A17 DDID_TXN1
B17 DDID_TXP1

bga1364-intel-genuine

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EDP_AUXN
EDP_AUXP
EDP_HPD
EDP_TXN0
EDP_TXN1
EDP_TXP0
EDP_TXP1

EDP_RCOMP
EDP_DISP_UTIL

FDI_TXN0
FDI_TXP0
FDI_TXN1
FDI_TXP1

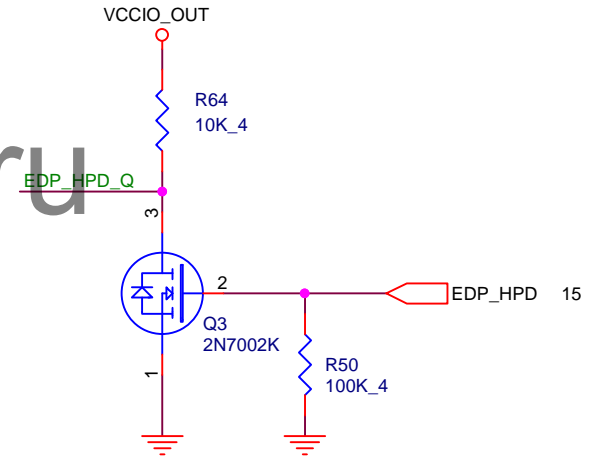
F15 EDP_AUXN 15
F14 EDP_AUXP 15
E14 EDP_HPD_Q


C14 EDP_TXN0 15
A12 EDP_TXN1 15
D14 EDP_TXP0 15
B12 EDP_TXP1 15

AG6 EDP_RCOMP R108 24.9/F 4 VCCIOA_OUT
E12

C12 FDI_TXN0 7
D12 FDI_TXP0 7
A14 FDI_TXN1 7
B14 FDI_TXP1 7

eDP_RCOMP
Trace length < 100 mils
Trace width = 20 mils
Trace spacing = 25 mils





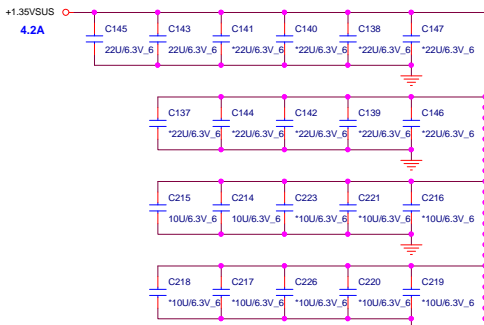
PROJECT : NL8
Quanta Computer Inc.

Size	Document Number	Rev
	Haswell 3/5 (DDI/eDP)	1A
Date:	Monday, March 10, 2014	Sheet 4 of 55

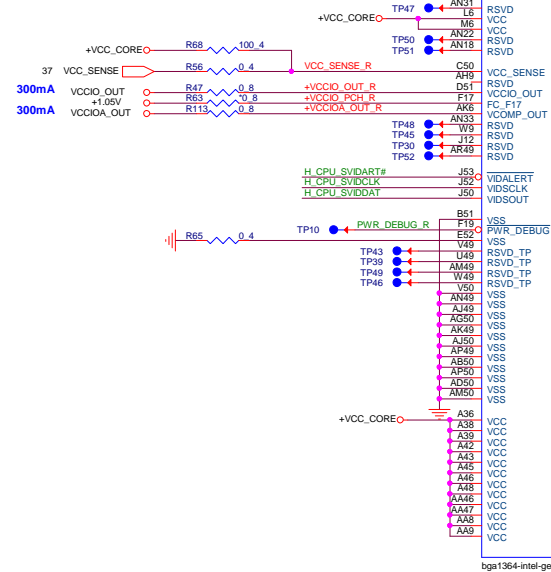
Haswell Processor (POWER)

2,13,14,34,41
6,37,41
2,4,37
2,10,11,35,40,41
+1.35VSUS
+VCC_CORE
+VCCIO_OUT
+1.05V
VCCIOA_OUT

05



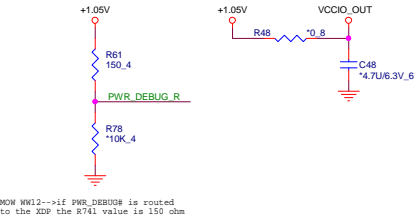
Capacitor	Value	Location
330uFx2	7343	BOT socket side
22uFx11	0805	5 on TOP, 6 on BOT inside socket cavity
10uFx10	0805	5 on TOP, 5 on BOT inside socket cavity



Capacitor	Value	Location
470uFx4	7343	TOP socket side
22uFx8	0805	4 on TOP, 4 on BOT near socket edge
22uFx11	0805	TOP, inside socket cavity
10uFx11	0805	BOT, inside socket cavity

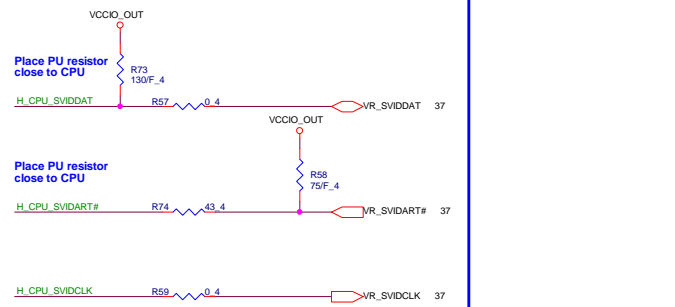
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Power Test Propose



SVID

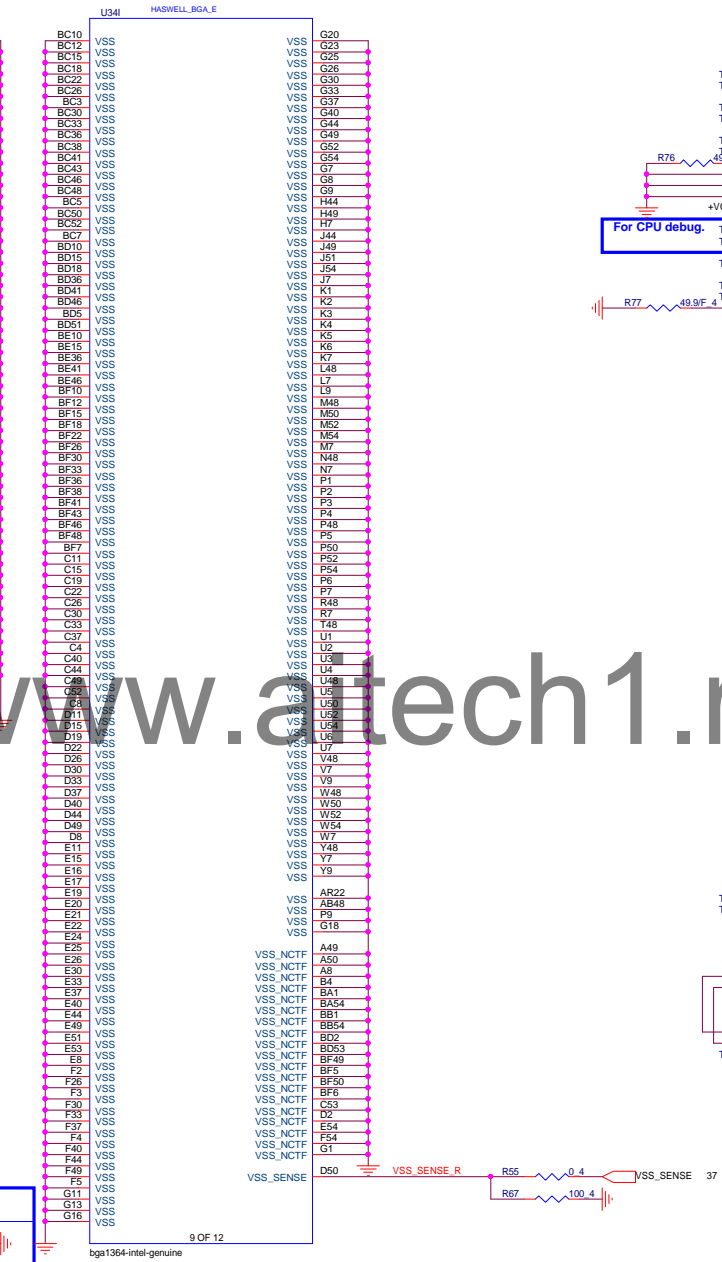
Layout note: need routing together and ALERT need between CLK and DATA.



Haswell Processor (GND)

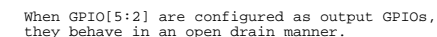
Haswell Processor (CFG,RSVD)

06

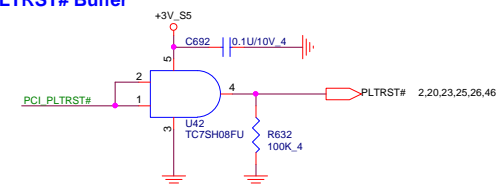
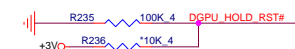


Configuration Signals:		The CFG signals have a default value of '1' if not terminated on the board.	
CFG[2]	PCI Express Static Lane Reversal	x1 = Normal operation x0 = Lane numbers reversed	CFG2 R102 1K 4
CFG[4]	eDP enable	x1 = Disabled x0 = Enabled	CFG4 R95 1K 4
CFG[6:5]	PCI Express Bifurcation	x00 = 1 x8 & 2 x4 PCI Express	CFG6 R91 *1K 4
		x01 = reserved	CFG5 R96 *1K 4
		x10 = 2 x8 PCI Express	
CFG[7]	PEG defer training	x1 = PEG train follow RESETB de-asserted	CFG7 R93 *1K 4
		x0 = PEG wait for BIOS fro training	

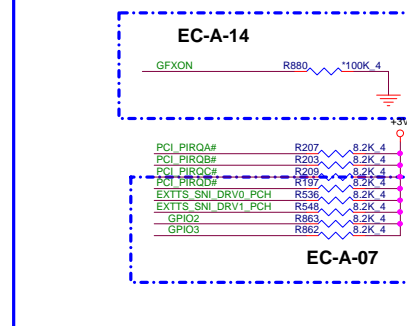
07



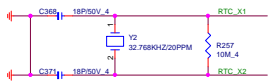
(US) 

GPIO50
DGPU_HOLD_RST# R

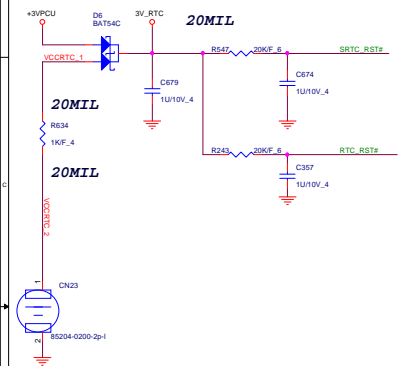
PCI PU



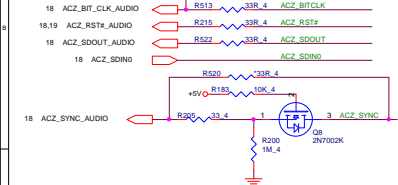
RTC Clock 32.768KHz (RTC)



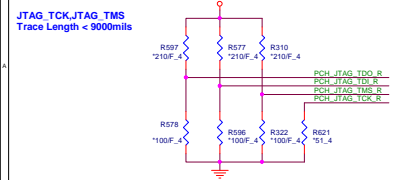
RTC Circuitry (RTC)



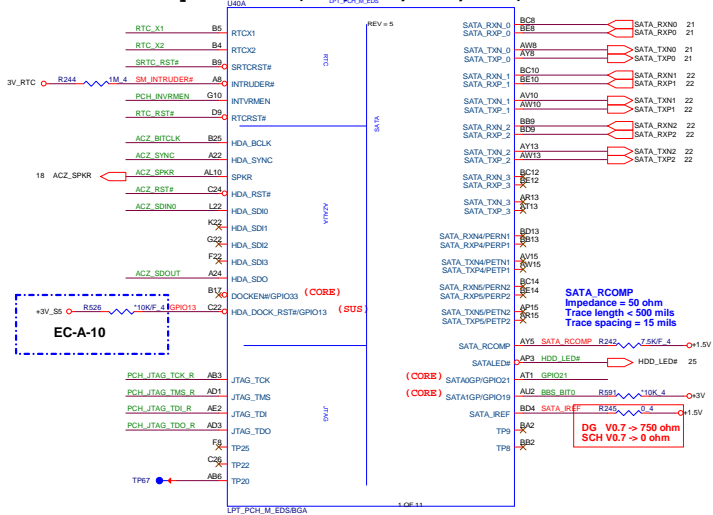
HDA



PCH JTAG



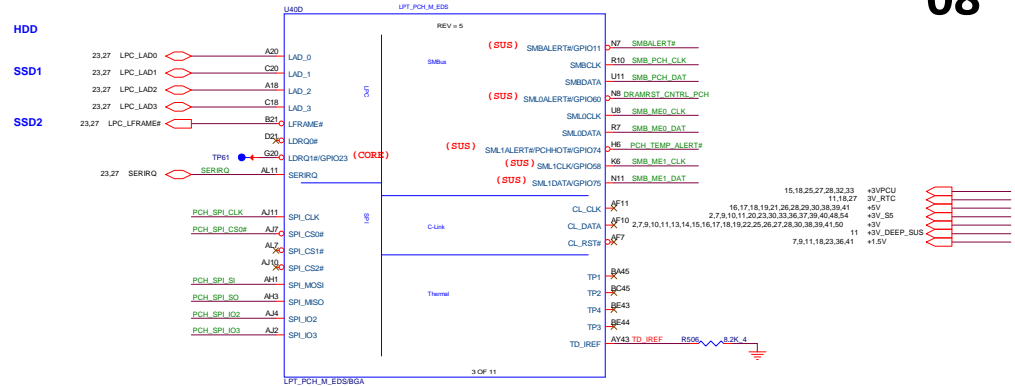
Lynx Point (RTC, I2HDA, SATA, JTAG)



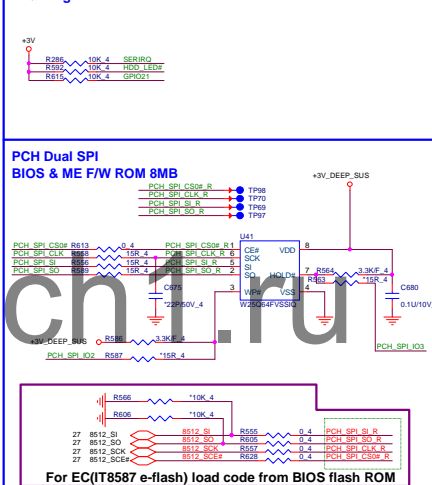
PCH STRAPPING

Pin Name	Usage	Sampled	Configuration	Circuitry
SPKR	No Reboot	PWROK	0 = Disable (Int PD) 1 = Enable	ACZ_SPKR R285 *1K_4 -> 3V
GPIO62 / SUSCLK	PLL On-Die Voltage Regulator Enable	RSMRST#	0 = Disable 1 = Enable (Int PU)	7 SUSCLK R253 *1K_4
GPIO55	Top-Block Swap Override	PWROK	0 = Top-Block Swap mode 1 = Default (Int PU)	7 STP_A60V/R R245 *1K_4
INTVRMEN	Integrated VRM Enable	Always	0 = Disable 1 = Enable	PCH_INVRMEN R565 *33K_4 -> 3V_RTC
GPIO51	Boot BIOS Strap bit 1	PWROK	0 = Disable 1 = Enable	7 BIOS_BIT1 R235 *1K_4
SATA1GP/GPIO19	Boot BIOS Strap bit 0	PWROK	0 = Disable 1 = Enable	7 BIOS_BIT0 R234 *1K_4
HDA_SDO	Flash Descriptor Security Override / Intel ME Debug Mode	PWROK	0 = Security Effect (Int PD) 1 = Can be Overrid	ACZ_SDO_HDA_IO R231 *1K_4 -> VCC_HDA_IO
GPIO36	RSVD	PWROK	Internal PD	10 GPIO36 R573 *1K_4 -> 3V
SATA3GP/GPIO37	TLS Confidentiality	PWROK	0 = TLS no confidentiality (Int PD) 1 = TLS with confidentiality	10 FDL_OVRVLG R575 *1K_4 -> 3V
GPIO8	RSVD	RSMRST#	Internal PU	10,23 BT_OFF# R321 *1K_4
GPIO28	PLL on die VR enable	RSMRST#	0 = Disable 1 = Enable (Int PU)	10 PLL_OVRV_EN R231 *1K_4
DSWVREN	On Die DSW VR Enable	Always	0 = Enable 1 = Disable	7 DSWVREN R560 *33K_4 -> 3V_RTC
HDA_SYNC	On-Die PLL VR Voltage Select	RSMRST	0 = Support by 1.8V (weak pull-down) 1 = Support by 1.5V	+VCC_HDA_IO R201 *1K_4 ACZ_SYNC

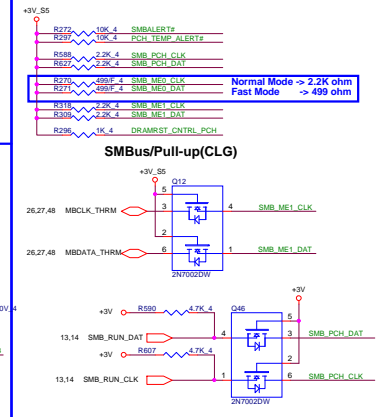
Lynx Point (LPC, SPI, SMBUS, C-LINK, THERMAL)



Pull High



SMBus



Lynx Point (PCIE,USB3.0,USB2.0)

LPT_PCH_M_EDS

U400

AW31

AY31

BE32

BC32

AT31

AR31

BD33

BB33

PETN2/USB3TN4

PETP2/USB3TP4

AW33

AY33

BE34

BC34

AT33

AR33

BE36

BC36

AW36

AY36

BD37

BB37

PETN.5

PETP.5

AY38

AW38

BE38

BC38

AT38

AR38

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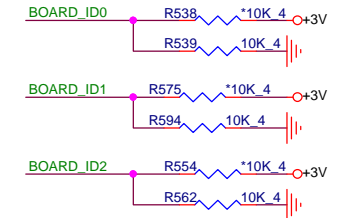
BC38

Lynx Point (GPIO,CPU/MISC,NCTF)

2,7,8,9,11,13,14,15,16,17,18,19,22,25,26,27,28,30,33,36,37,39,40,48,54
+3V
+1.05V
+3V_S5

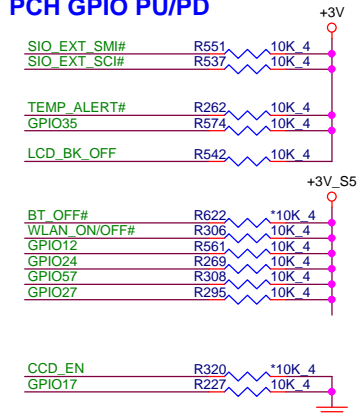
10

BOARD ID SETTING



BOARD_ID[3:0]			Model Name
BOARD ID0	BOARD ID1	BOARD ID2	B Note
0	0	0	SDV
0	0	1	SIV
0	1	0	SIT
0	1	1	SVT
1	0	0	SOVP
1	0	1	
1	1	0	
1	1	1	

PCH GPIO PU/PD

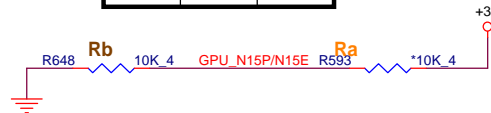


PCH MISC PU/PD



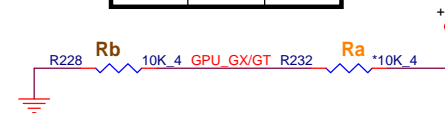
NL8 GPU N15P/N15E Select setting

GPIO16	N15P	N15E
Stuff	Ra (Hi)	Rb (Lo)



NL8 GPU GX/GT Select setting

	GX	GT
Stuff	Ra (Hi)	Rb (Lo)



BIOS RECOVERY

0 = Enable
1 = Disable

Swap GPIO

0 = SGPIO
1 = Default

MFG TEST

SV Detect

0 = SV Detect
1 = Default

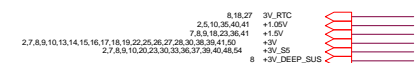
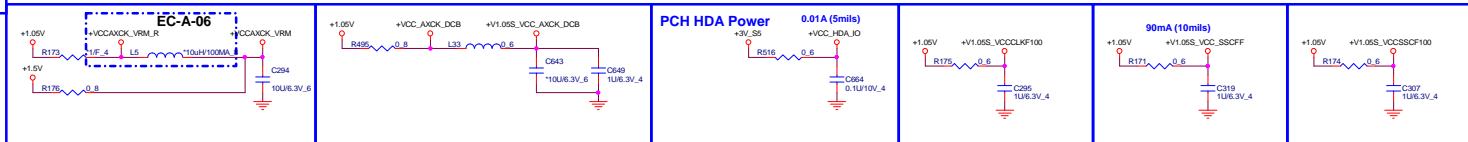
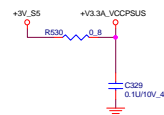
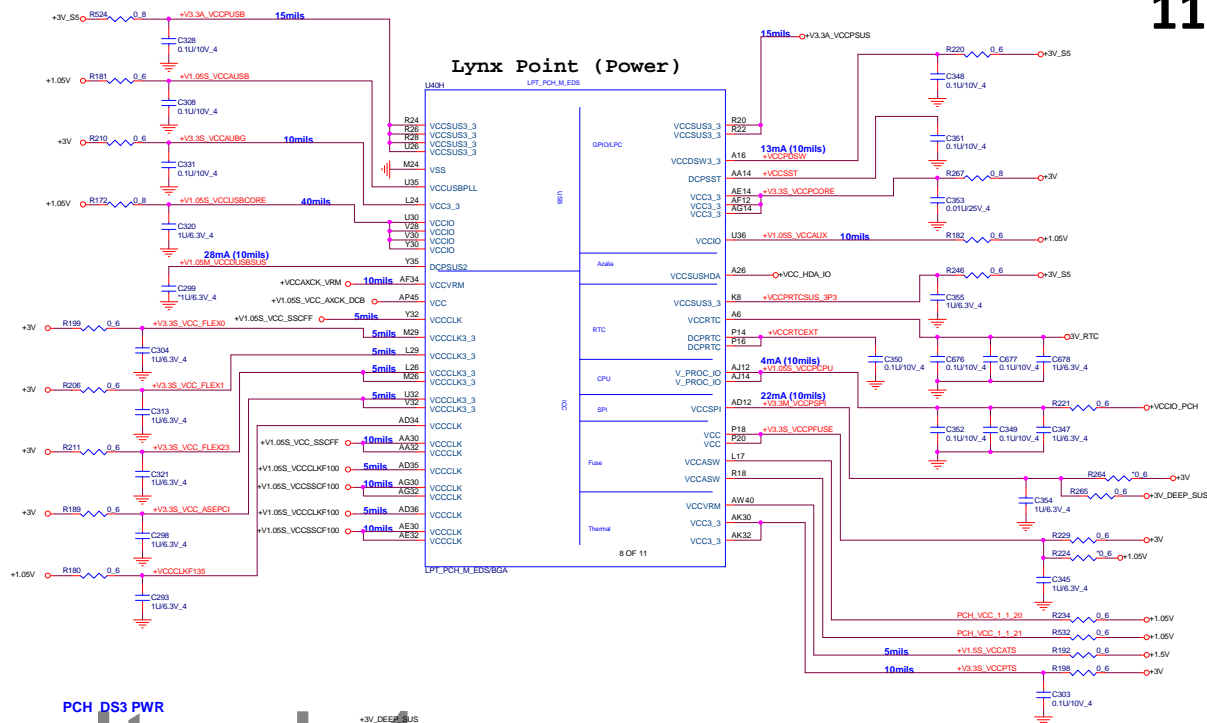
BIOS_RESP

0 = BIOS RESP
1 = Default

PROJECT : NL8
Quanta Computer Inc.

Size: Document Number: LPT 4/6 (GPIO/MISC) Rev: 1A

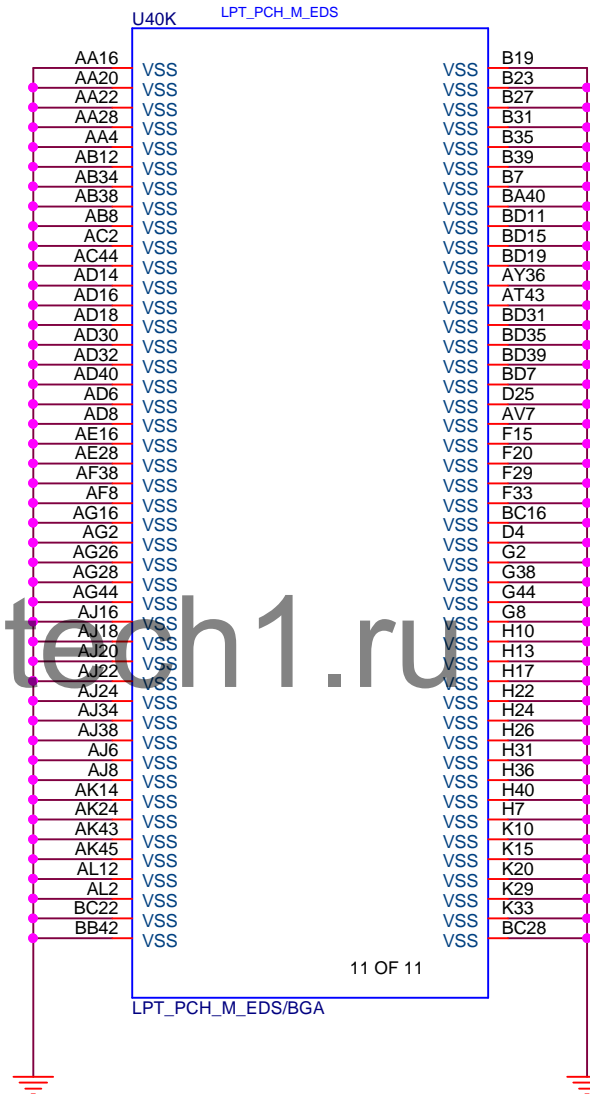
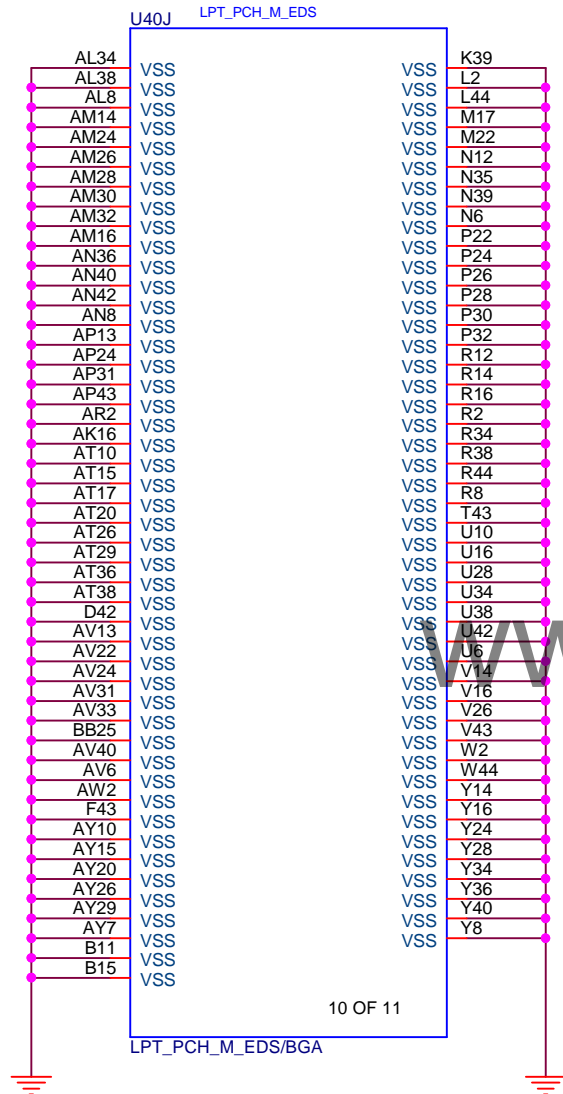
Date: Monday, March 10, 2014 Sheet: 10 of 55



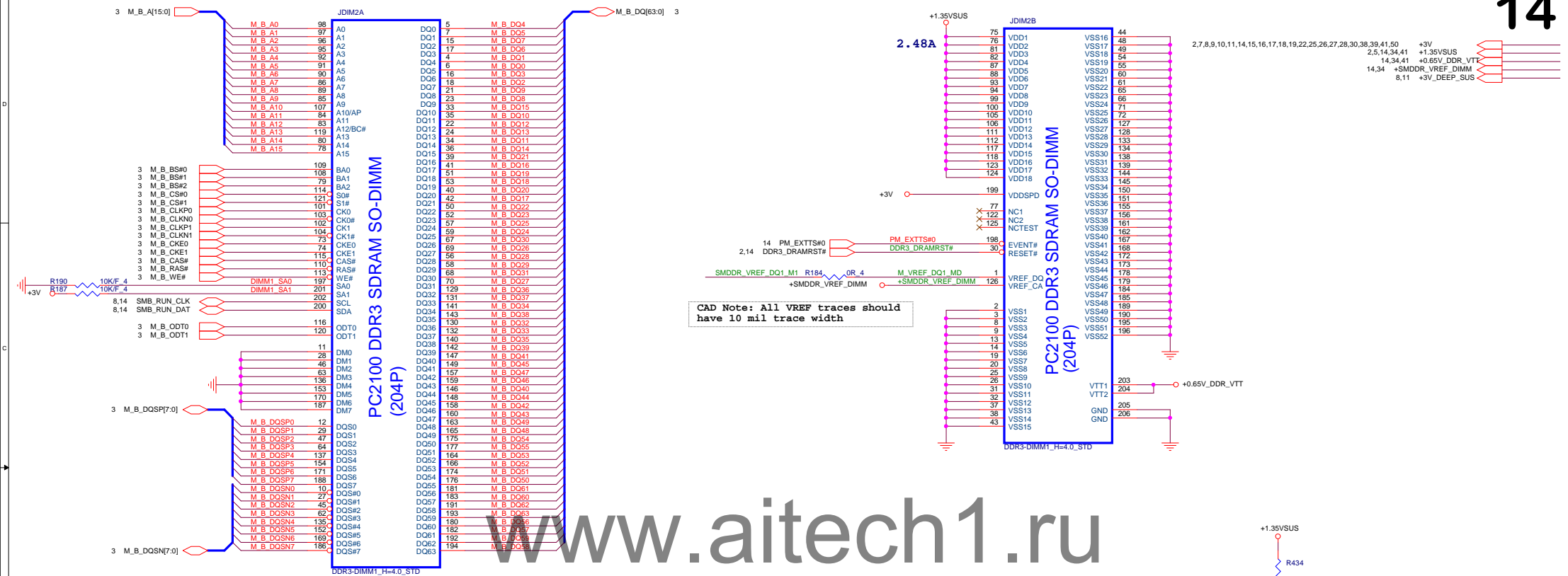
Lynx Point (GND)

Lynx Point (GND)

12



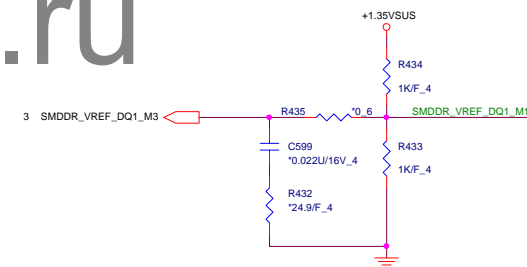
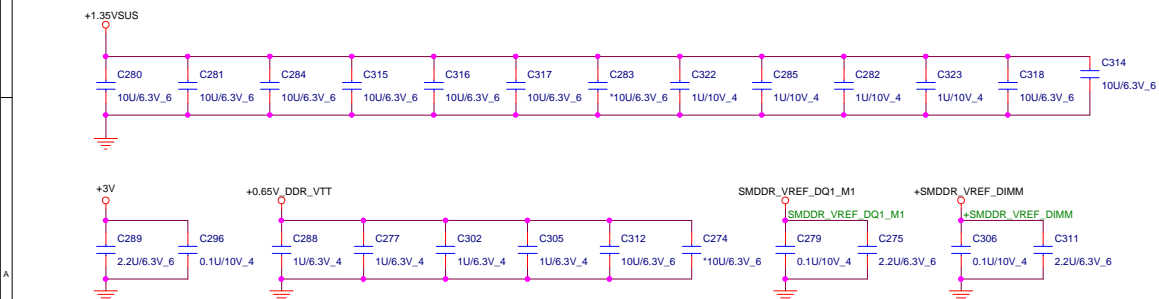
DDR_STD(DDR)



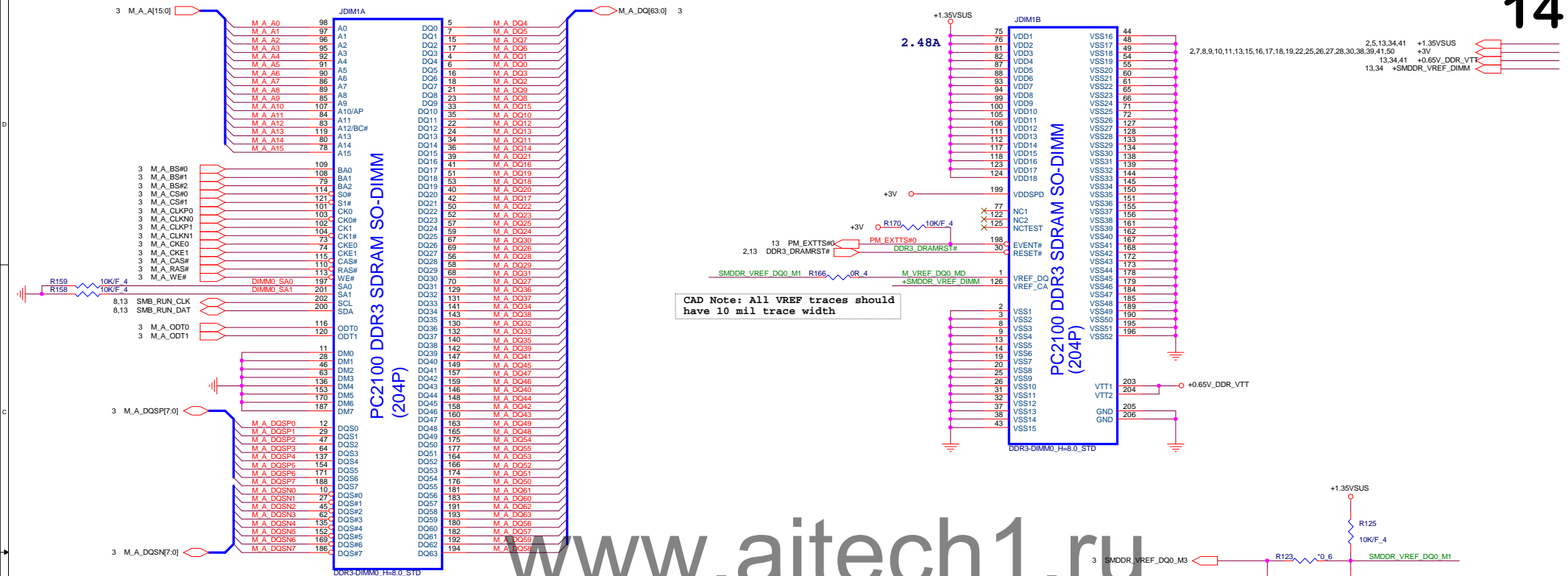
M.B.DQ60
M.B.DQ62
M.B.DQ63
M.B.DQ66
M.B.DQ67
M.B.DQ68
M.B.DQ69

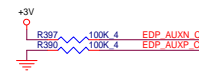
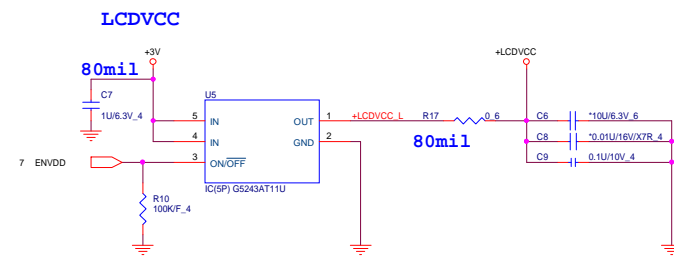
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Place these Caps near SO-Dimm1

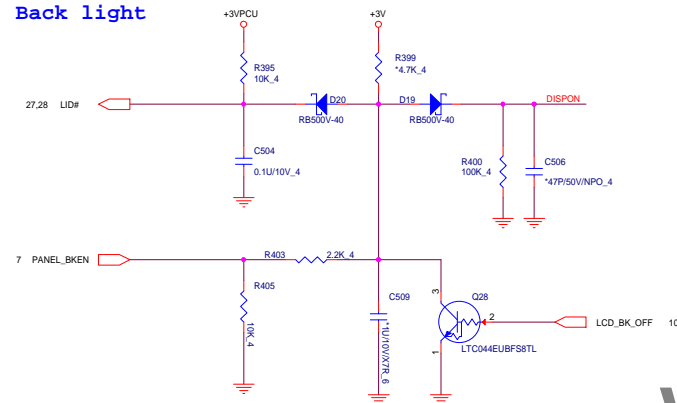


DDR_STD (DDR)

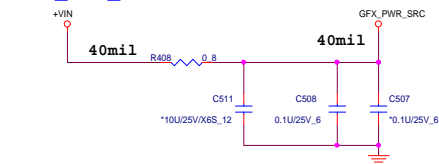




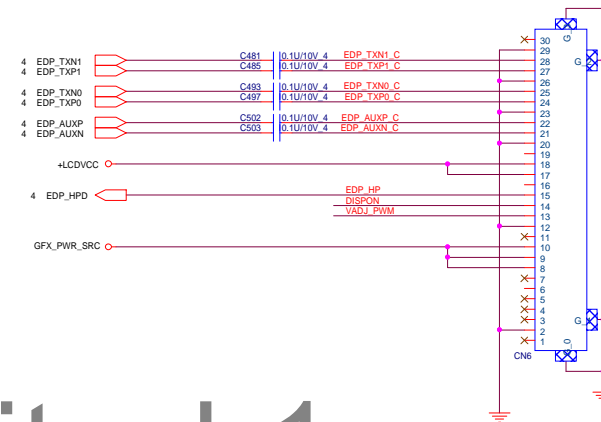
Back light



GFX_PWR_SRC

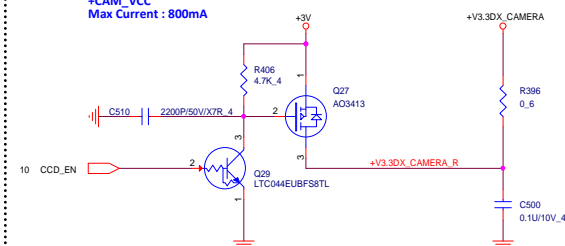


30Pin eDP CN

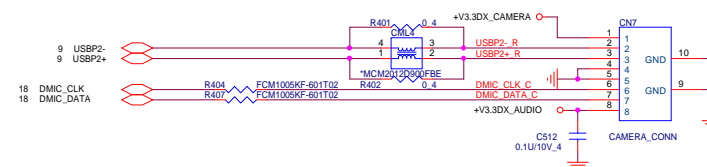


CAMERA VCC Control

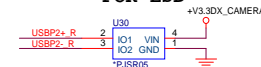
+CAM_VCC
 Max Current : 800mA

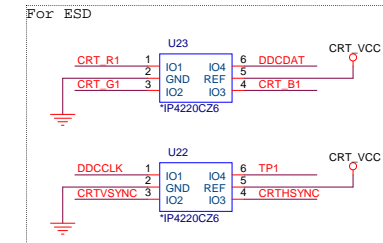
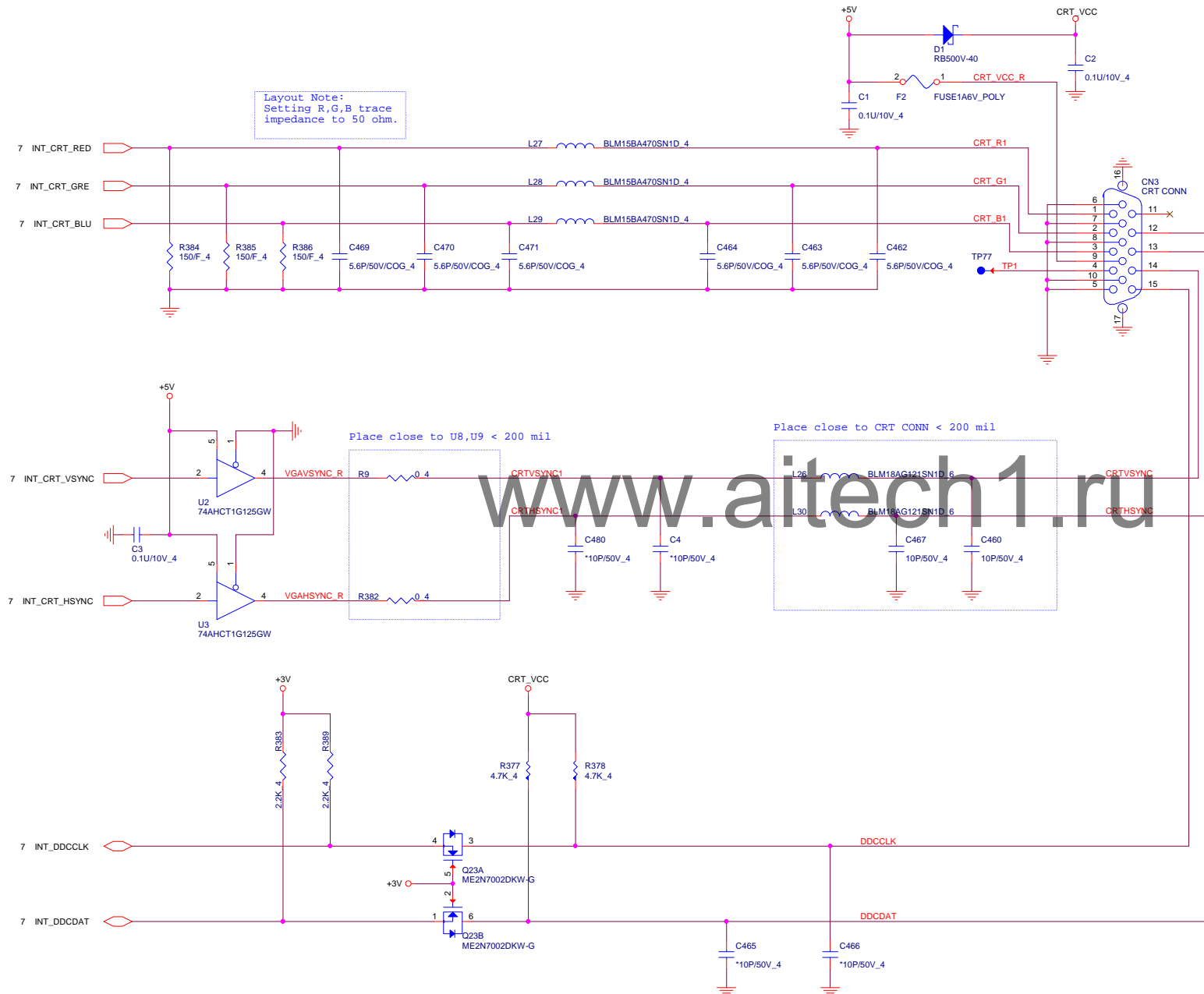


CAMERA/DMIC CONN



FOR ESD

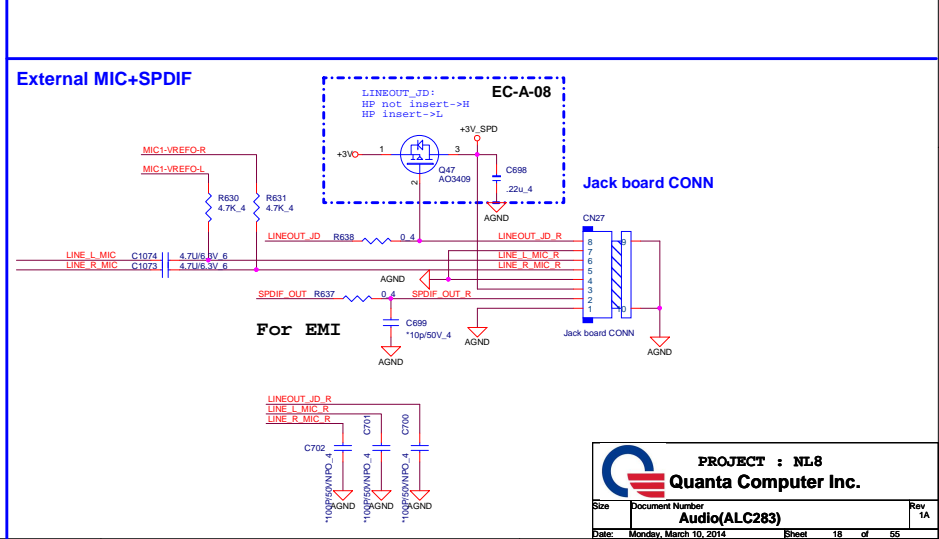
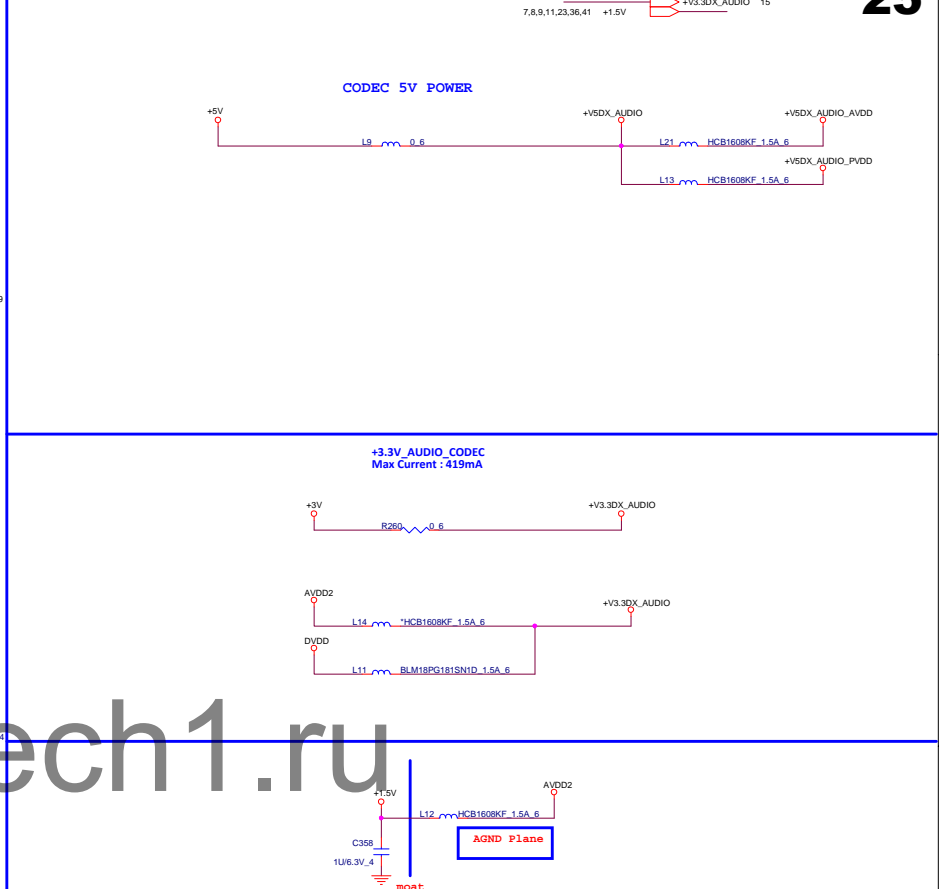






Layout note:Place close to HDMI Conn

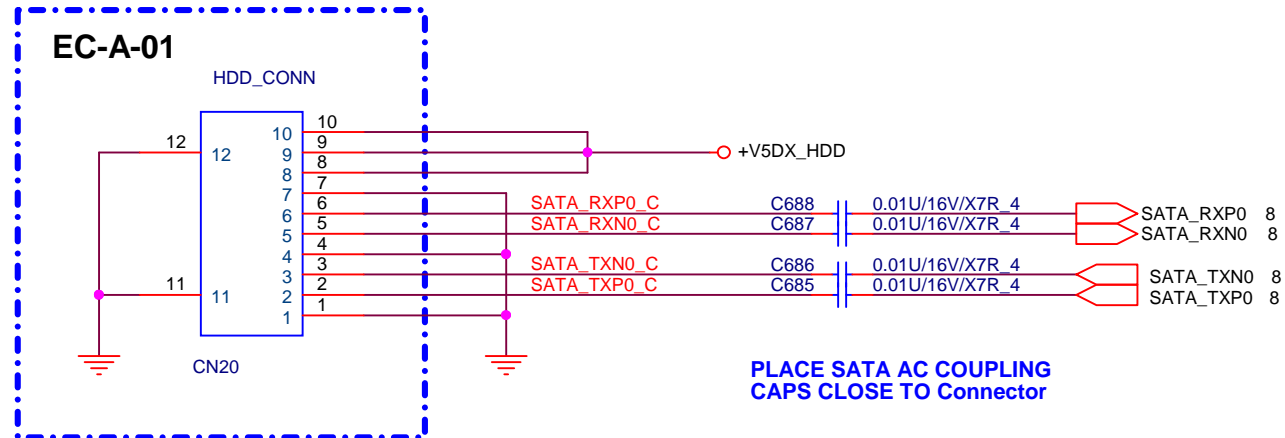




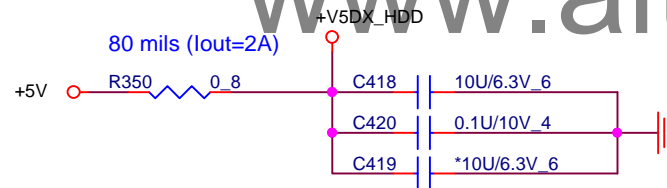



R364	R363	R373	R372	Gain(Differential)
NC	NC	0	0	11dB
0	NC	NC	0	14dB
NC	0	0	NC	19dB
0	0	NC	NC	25dB

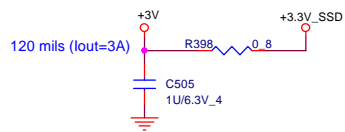




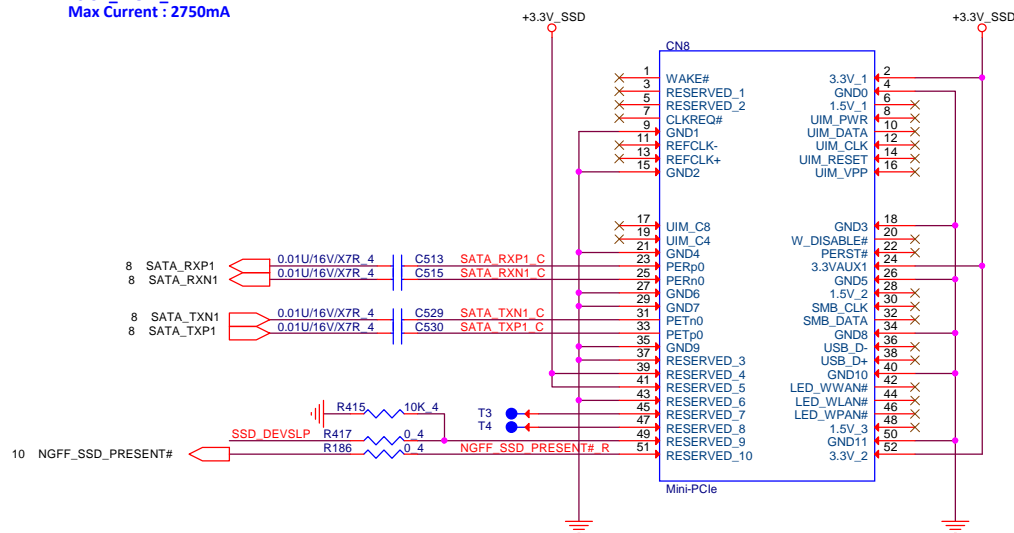
DC Current rating: 2 A (MAX)



 PROJECT : NL8 Quanta Computer Inc.		
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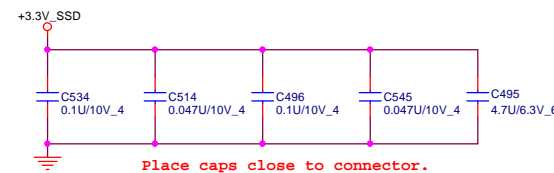
120 mils (Iout=3A)
+3.3V_NGFF_WWAN
Max Current : 2750mA



2,7,8,9,10,11,13,14,15,16,17,18,19,25,26,27,28,30,38,39,41,50 +3V

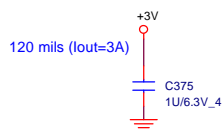


22

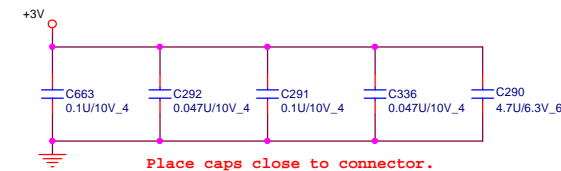
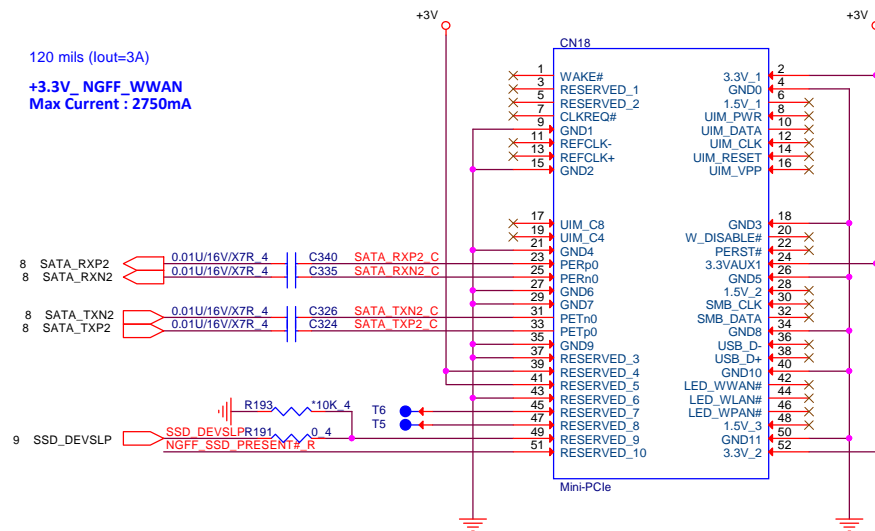


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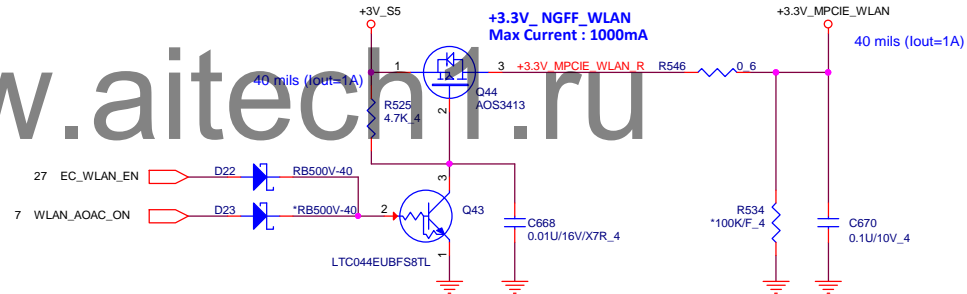
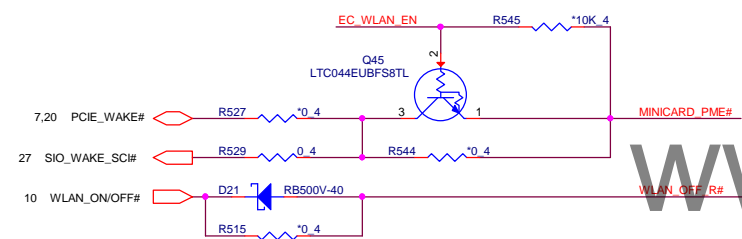
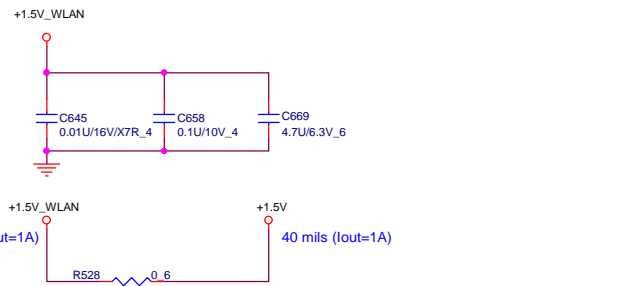
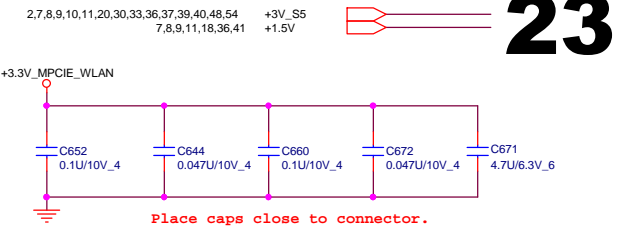
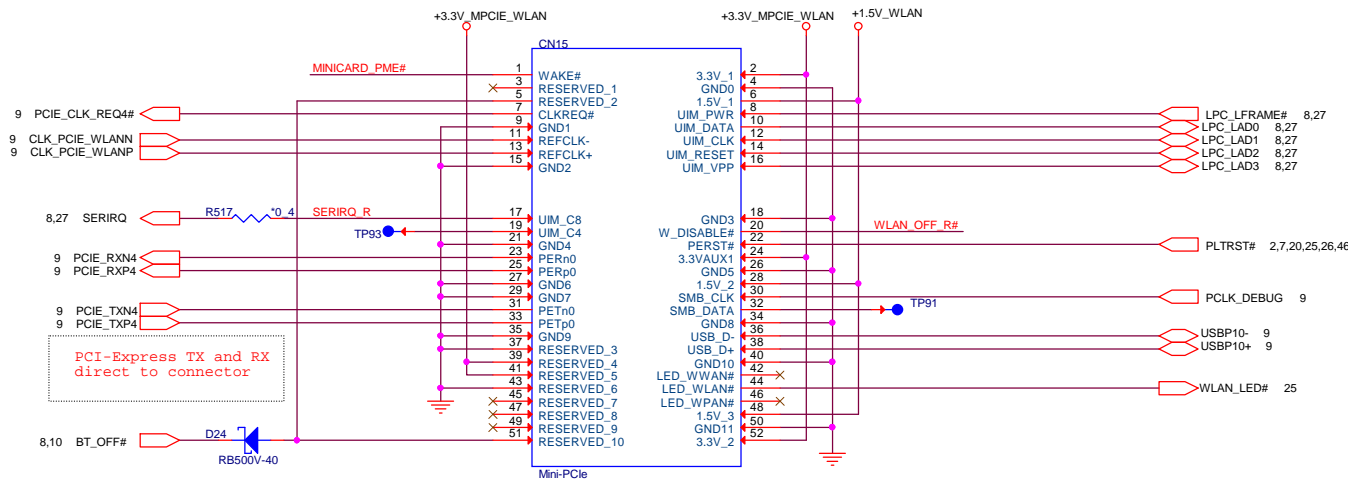
Mini-PCIE SSD connector

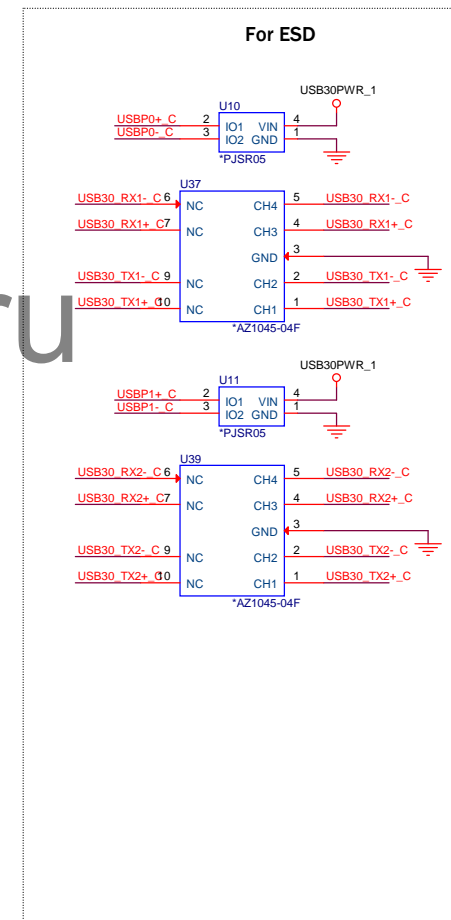
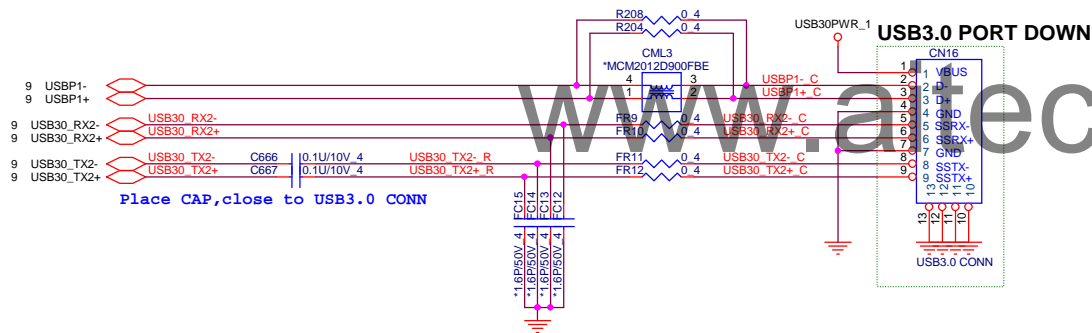
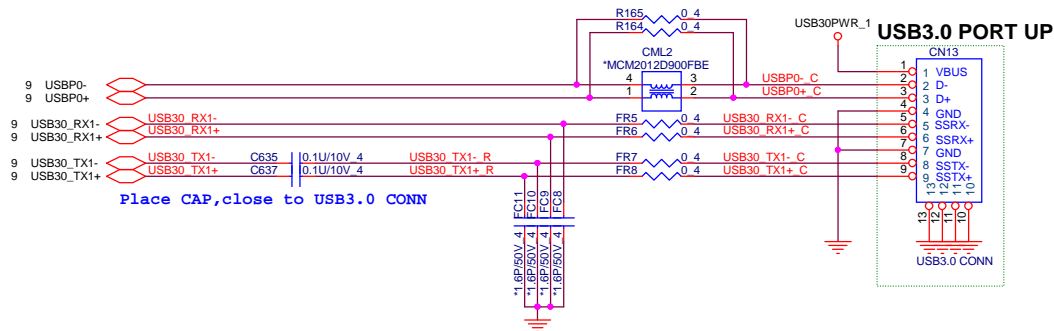
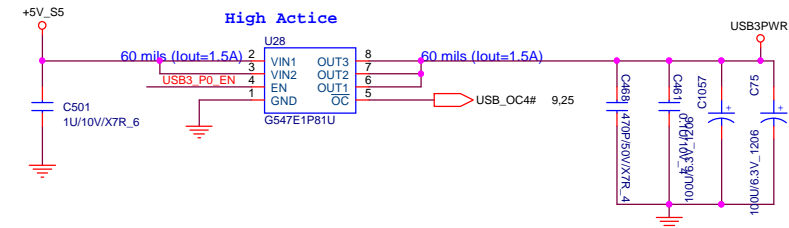
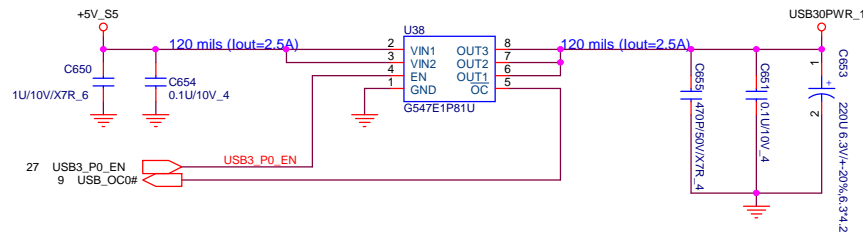


120 mils (Iout=3A)
+3.3V_NGFF_WWAN
Max Current : 2750mA



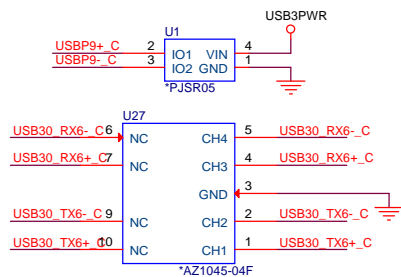
Mini PCIe Wifi/BT connector



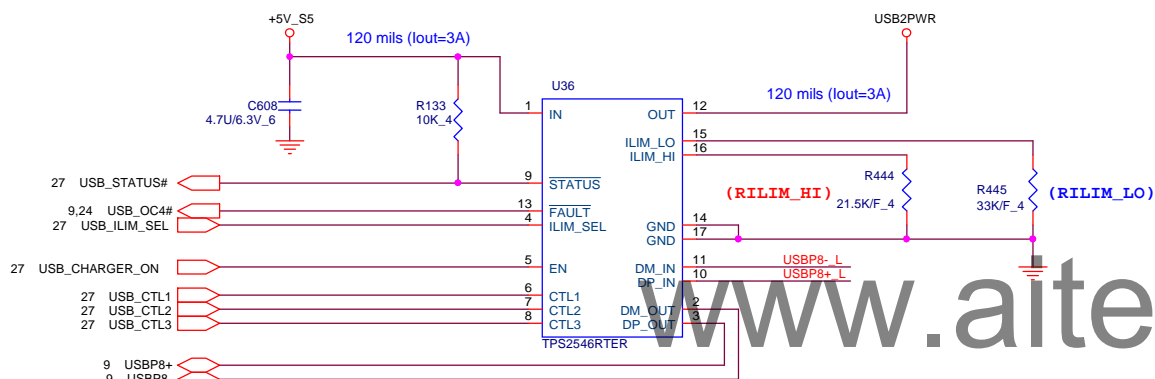


EC-A-17





USB Charger 2.0 Port



RILIM_LO is optional and the ILIM_LO pin may be left unconnected if the following conditions are met:

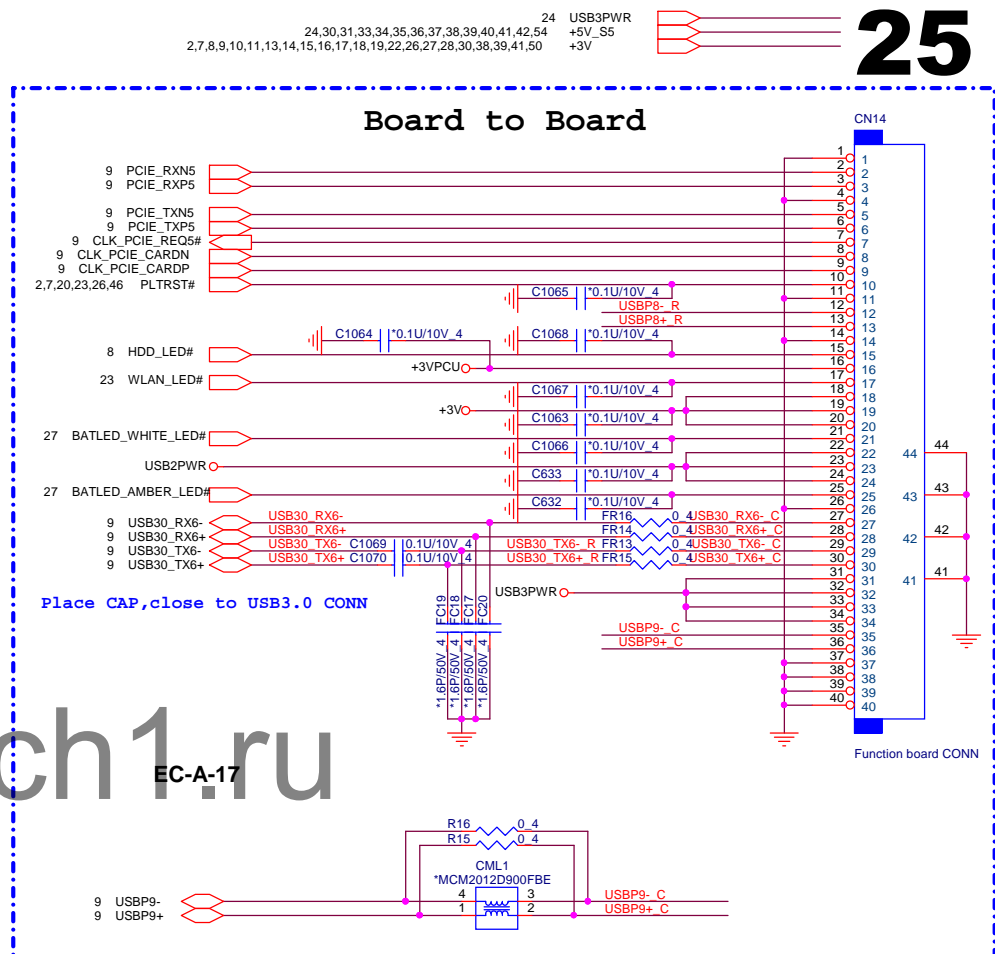
1. ILIM_SEL is always set high
 2. Load Detection - Port Power Management is not used
 3. Mouse / Keyboard wake function is not used
- If conditions 1 and 2 are met but the mouse / keyboard

The following equation determines the typical current limit:

The following equation programs the typical current limit:

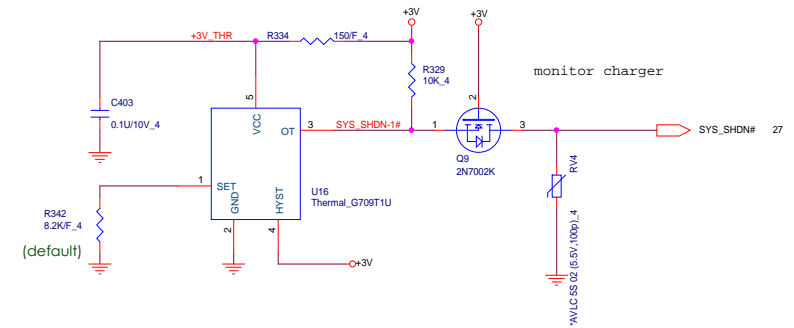
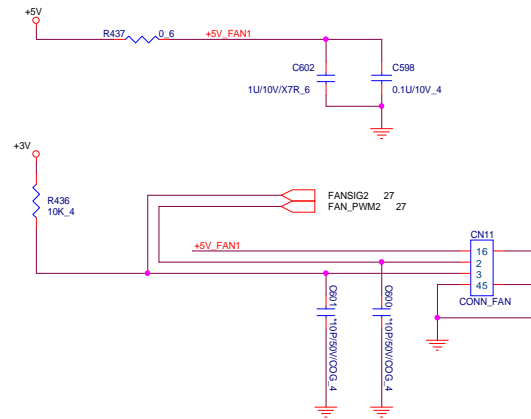
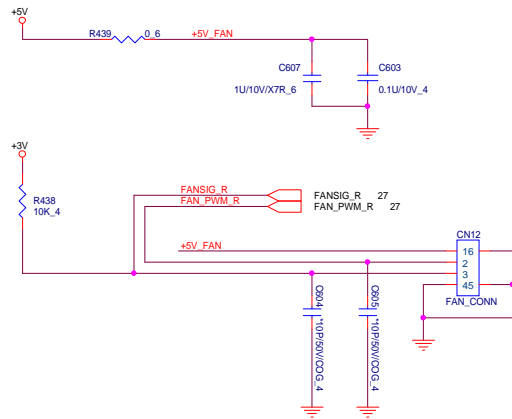
(1)
RILIM_XX corresponds to either RILIM_HI or RILIM_LO as appropriate.

$$I_{OS_typ}(mA) = \frac{50,500}{(R_{ILIM_xx}(k\Omega) + 0.1)}$$

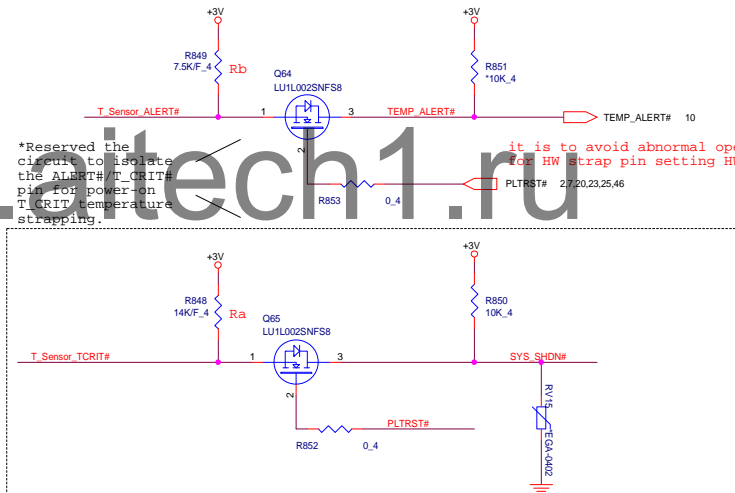
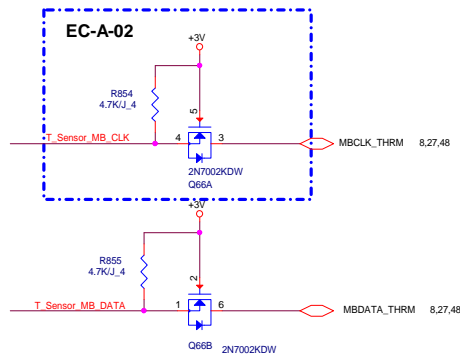
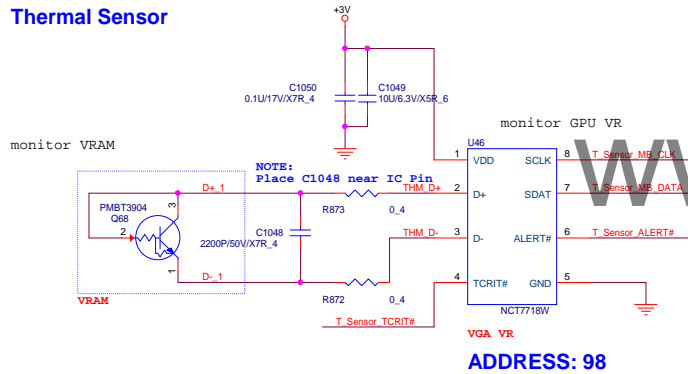


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Quanta Computer Inc.

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Thermal Sensor



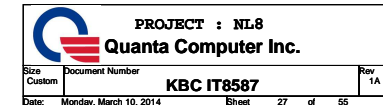
*Reserved the circuit to isolate the ALERT#/T_CRIT# pin for power-on T_CRIT temperature strapping.

it is to avoid abnormal operation when power on within 100ms for HW strap pin setting HW Shut-down Temp. 109 °C

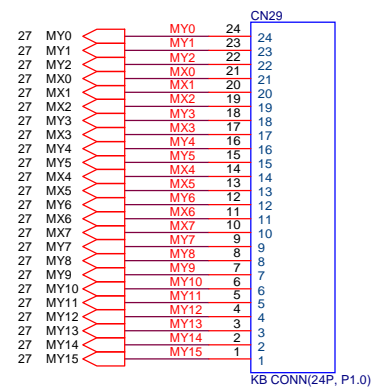
ALERT# /T_CRIT# Pull-up Resistor

	2Kohm	7.5Kohm	10.5Kohm	14Kohm	18.7Kohm
Rb	2Kohm	7.5Kohm	10.5Kohm	14Kohm	18.7Kohm
7.5Kohm	77°C	87°C	97°C	107°C	117°C
10.5Kohm	79°C	89°C	99°C	109°C	119°C
14Kohm	81°C	91°C	101°C	111°C	121°C
18.7Kohm	83°C	93°C	103°C	113°C	123°C
	85°C	95°C	105°C	115°C	125°C

T_CRIT temperature strapping point



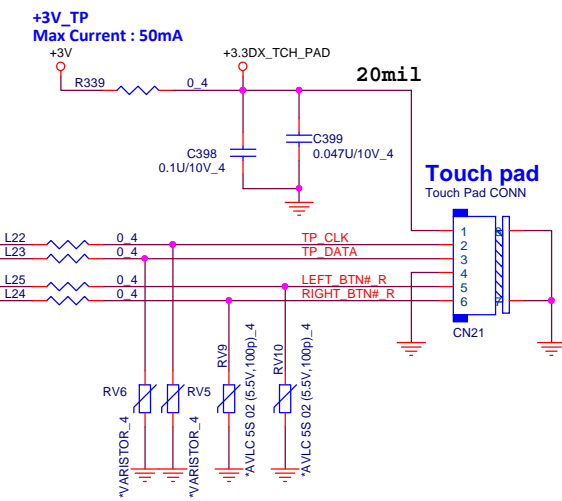
KEYBOARD



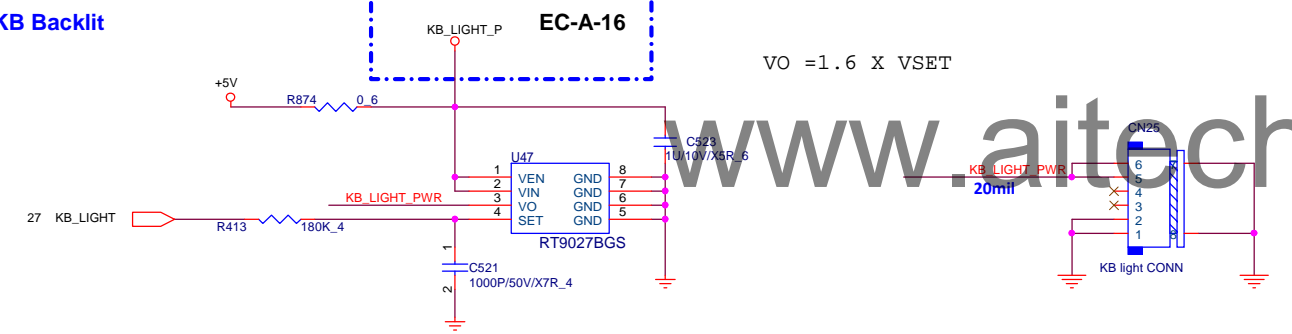
For EMI

MY15	C449	220P/50V/X7R_4	C447	220P/50V/X7R_4	MY13
MY10	C444	220P/50V/X7R_4	C446	220P/50V/X7R_4	MY12
MY11	C445	220P/50V/X7R_4	C456	220P/50V/X7R_4	MY3
MY14	C448	220P/50V/X7R_4	C438	220P/50V/X7R_4	MY6
MX0	C453	220P/50V/X7R_4	C454	220P/50V/X7R_4	MX1
MY1	C451	220P/50V/X7R_4	C440	220P/50V/X7R_4	MX7
MY5	C435	220P/50V/X7R_4	C439	220P/50V/X7R_4	MX6
MX3	C457	220P/50V/X7R_4	C443	220P/50V/X7R_4	MY9
MX2	C455	220P/50V/X7R_4	C442	220P/50V/X7R_4	MY8
MY0	C450	220P/50V/X7R_4	C441	220P/50V/X7R_4	MY7
MX5	C437	220P/50V/X7R_4	C434	220P/50V/X7R_4	MY4
MX4	C436	220P/50V/X7R_4	C452	220P/50V/X7R_4	MY2

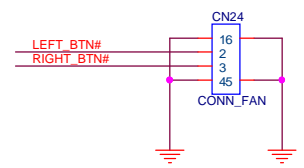
8,16,17,18,19,21,26,29,30,38,39,41 +5V
2,7,8,9,10,11,13,14,15,16,17,18,19,22,25,26,27,30,38,39,41,50 +3V
8,15,18,25,27,32,33 +3VPCU



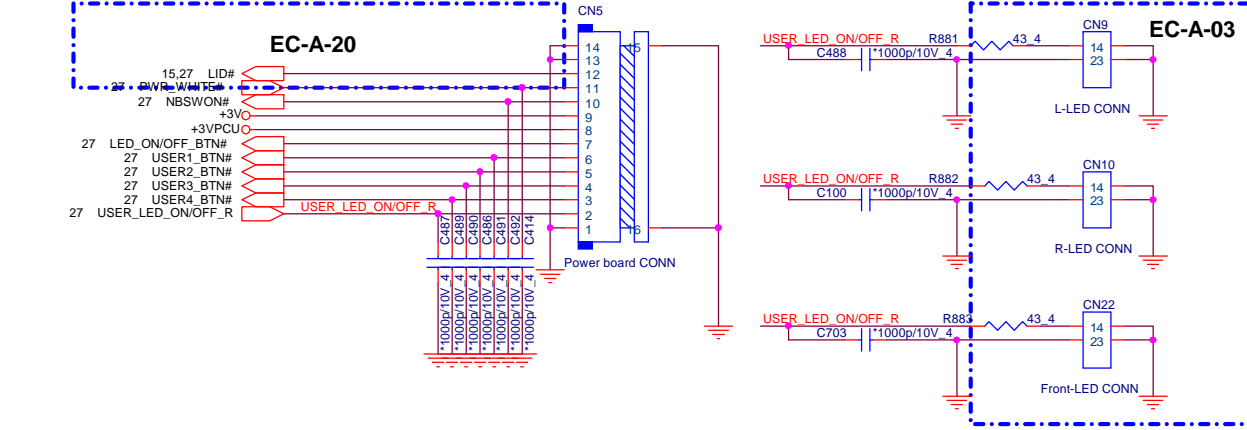
KB Backlit



Touch button connector



Power board



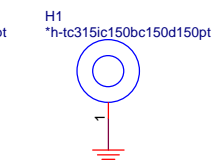
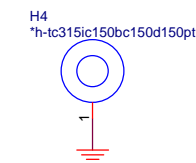
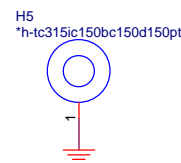
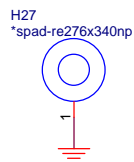
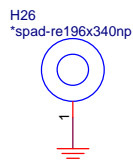
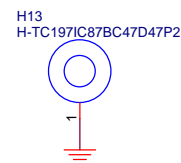
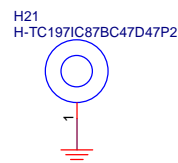
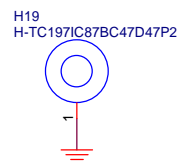
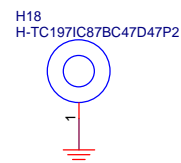
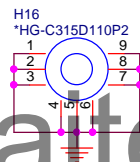
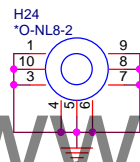
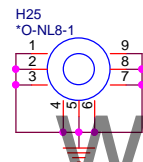
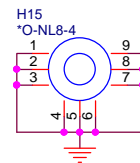
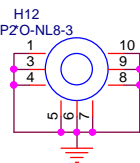
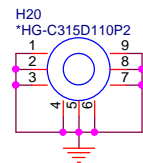
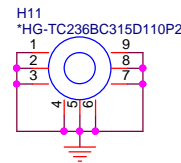
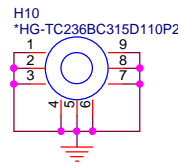
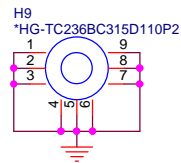
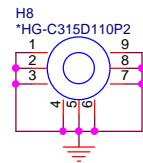
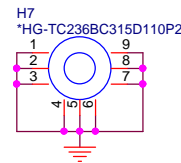
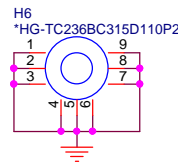
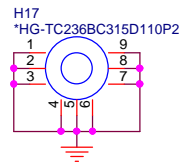
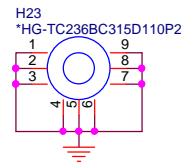
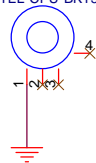
EC-A-20



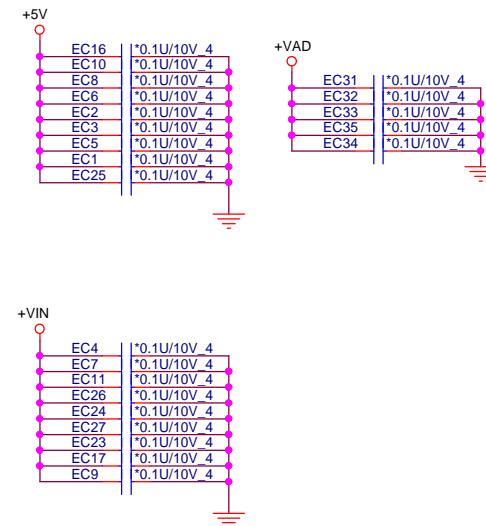
CPU BRACKET

INTEL-CPU-BKT3

H3
*INTEL-CPU-BKT3

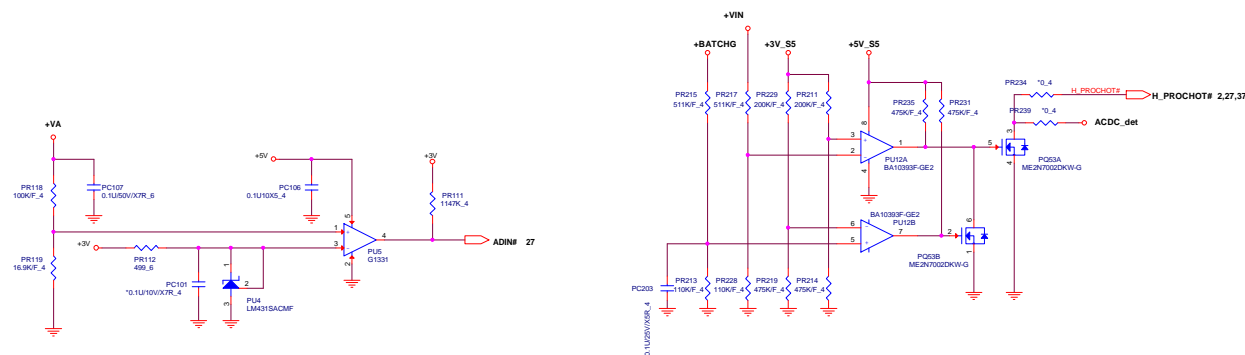


EMI

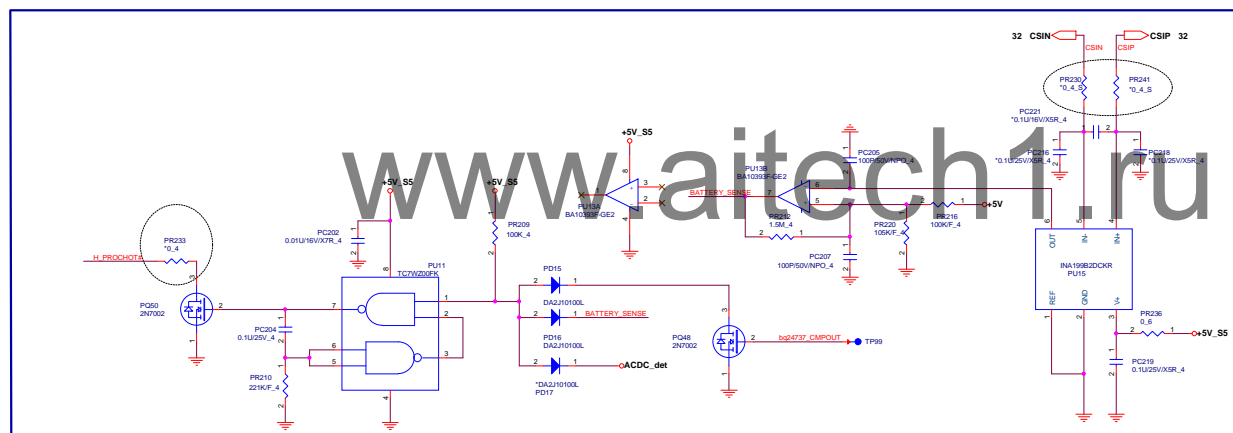


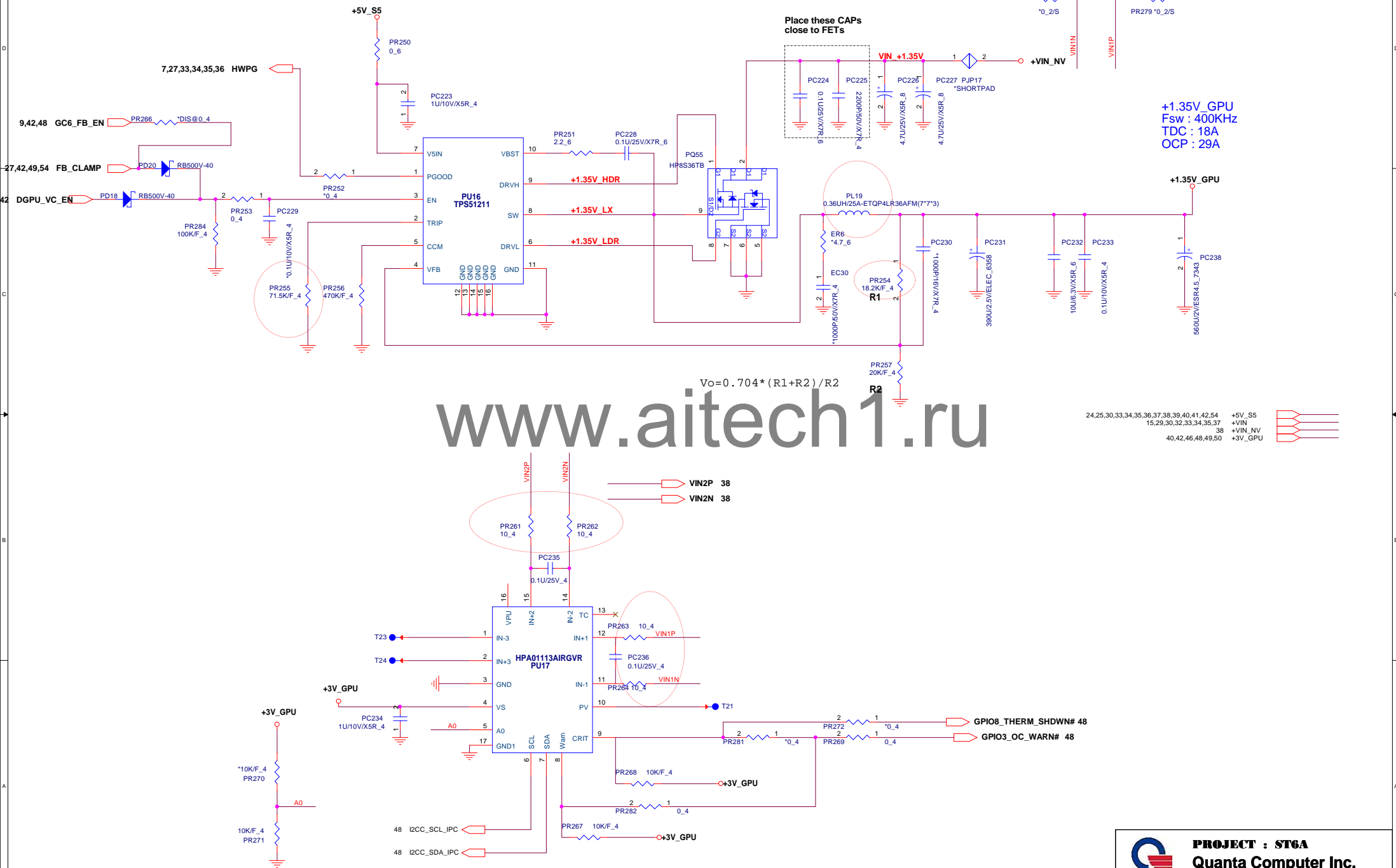
ESD



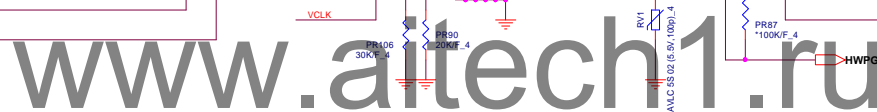


10ms one-shot circuit

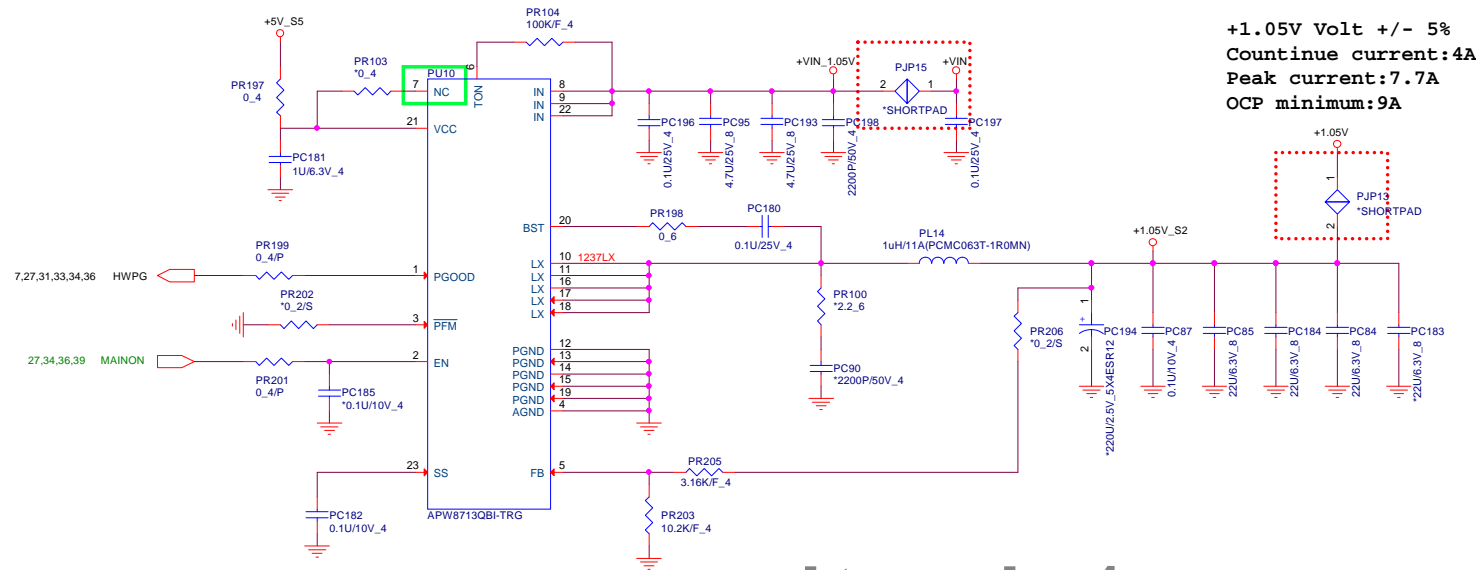




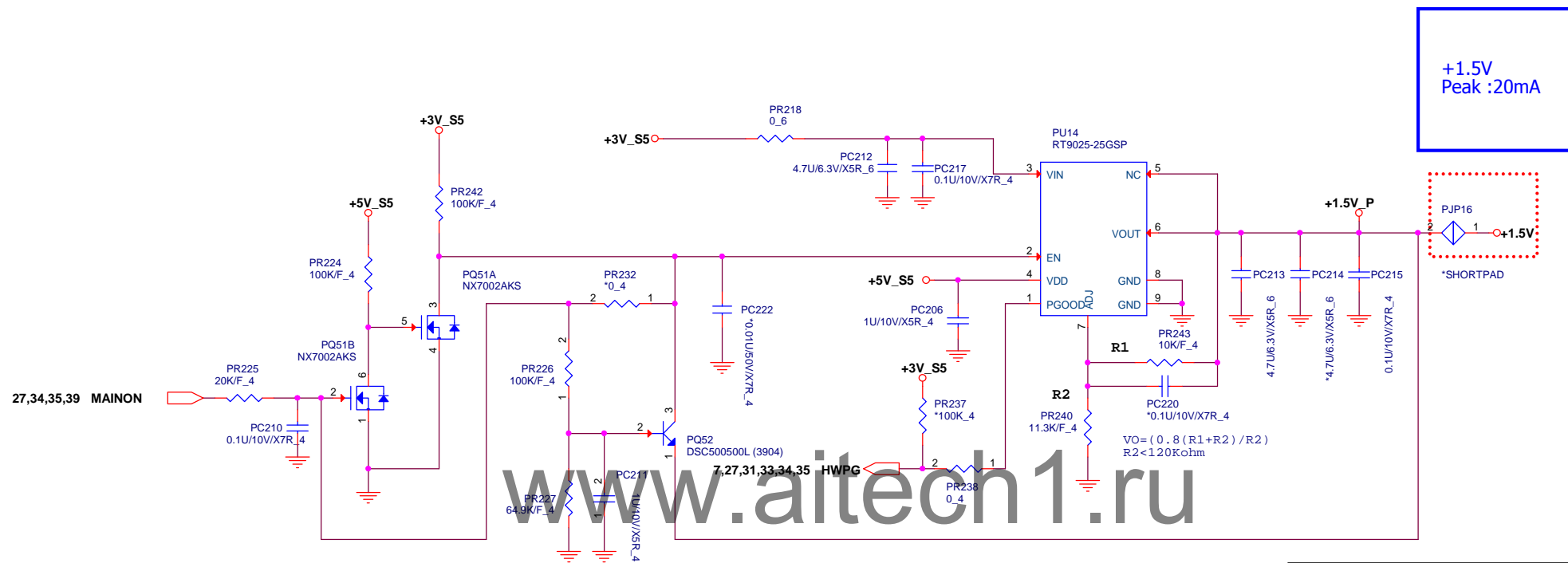









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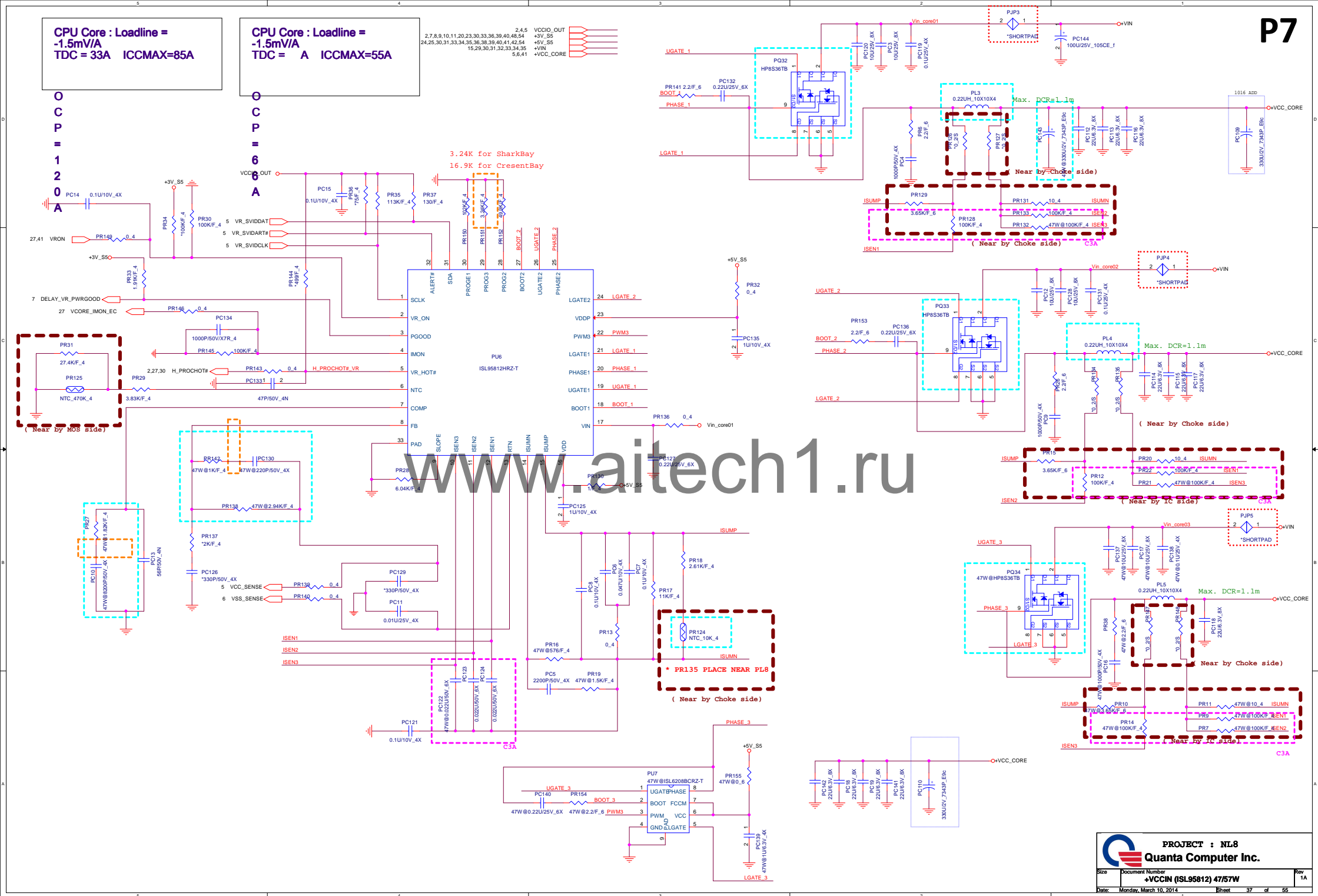


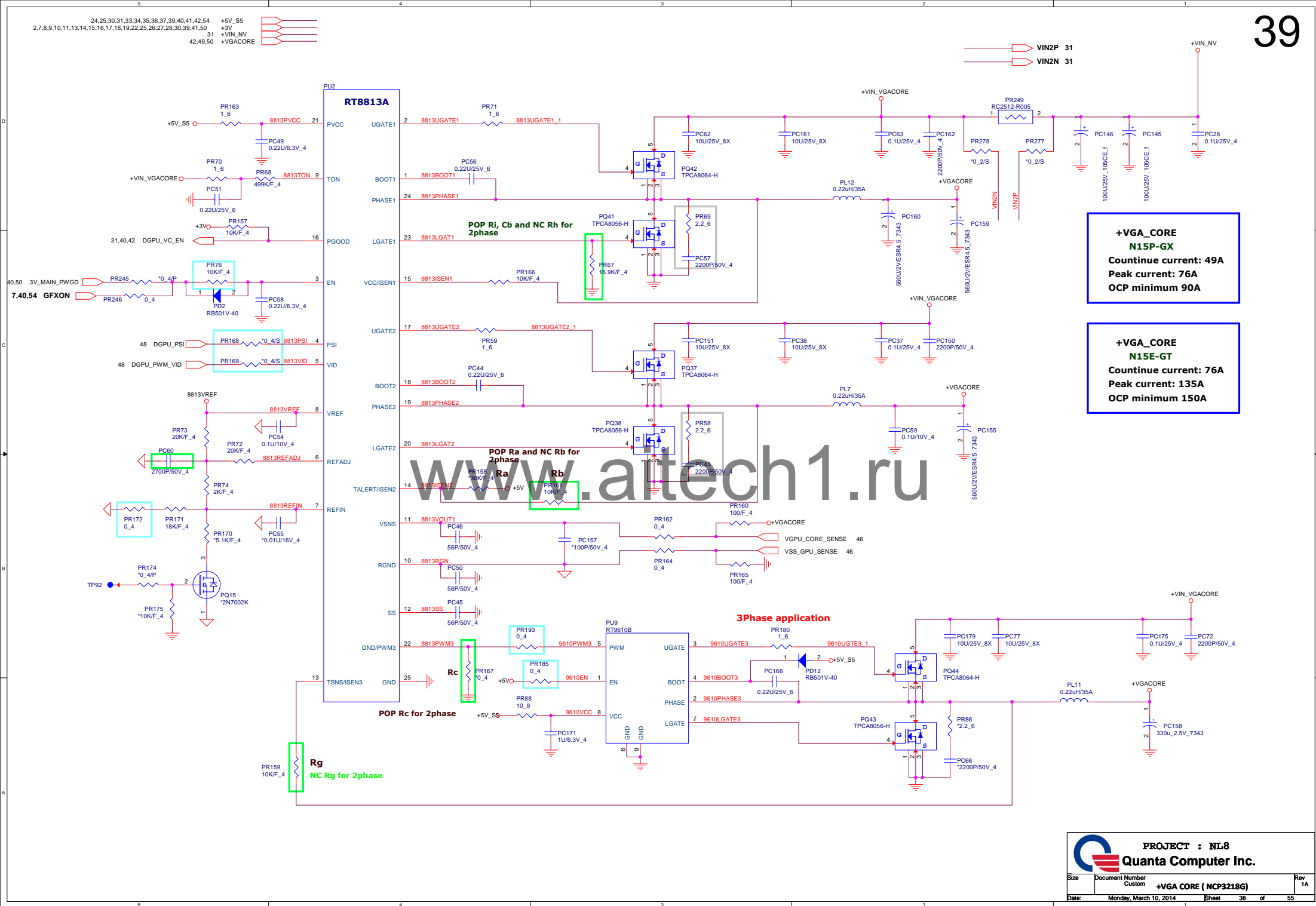
 PROJECT : NL8 Quanta Computer Inc.		
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CPU Core : Loadline =
-1.5mV/A
TDC = A ICCMAX=55A

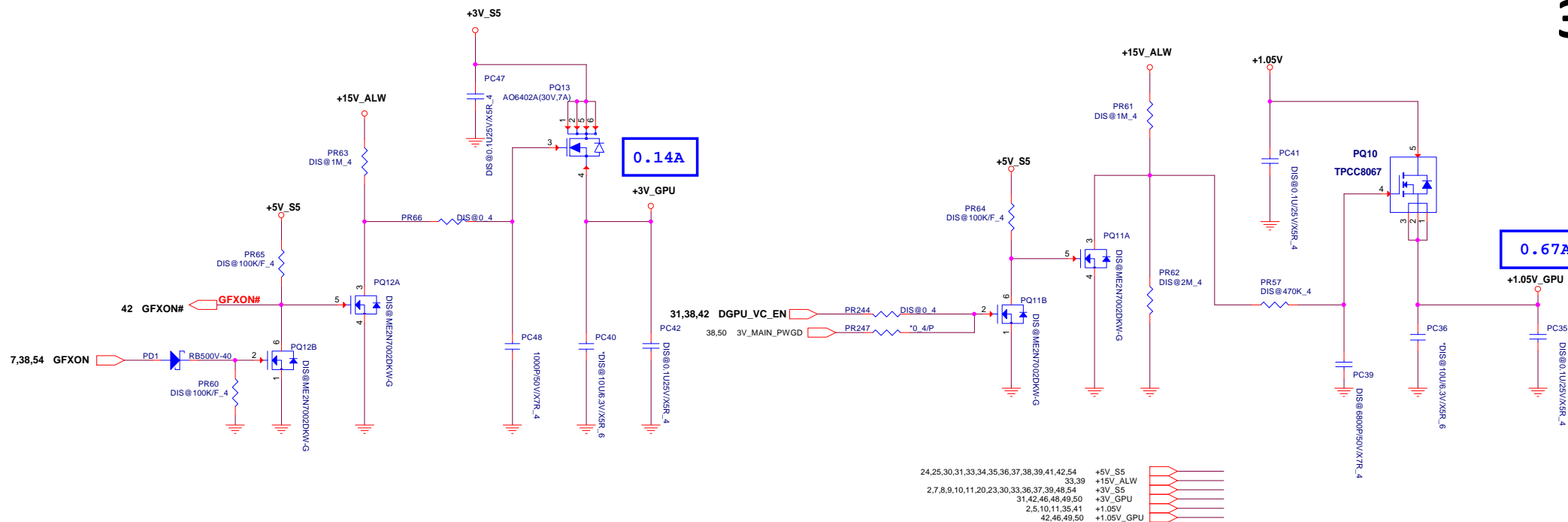
	2,4,5	VCCIO_OUT	
2,7,8,9,10,11,20,23,30,33,36,39,40,48,54		+3V_S5	
24,25,30,31,33,34,35,36,38,39,40,41,42,54		+5V_S5	
15,29,30,31,32,33,34,35		+VIN	
5,6,41		+VCC_CORE	

P7



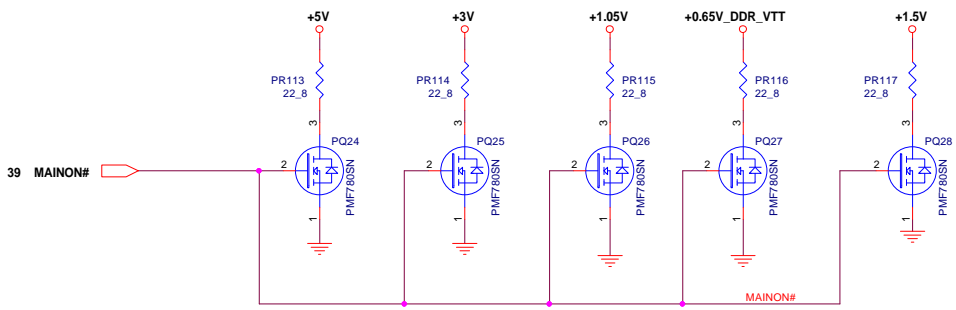




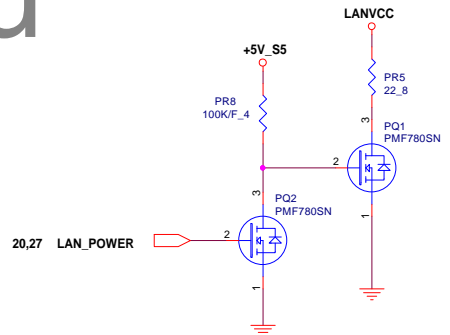
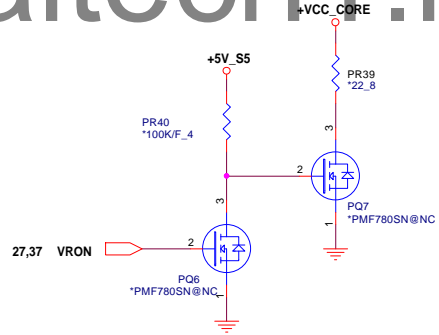
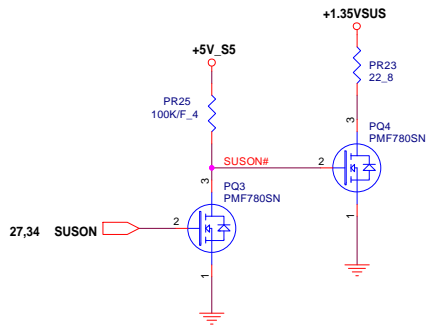


DISCHARGE

8,16,17,18,19,21,26,28,29,30,38,39	+5V
2,7,8,9,10,11,13,14,15,16,17,18,19,22,25,26,27,28,30,38,39,50	+3V
2,5,10,11,35,40	+1.05V
13,14,34	+0.65V_DDR_VTT
7,8,9,11,18,23,36	+1.5V
2,5,13,14,34	+1.35VSUS
24,25,30,31,33,34,35,36,37,38,39,40,42,54	+5V_S5
5,6,37	+VCC_CORE
20	LANVCC

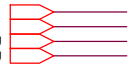


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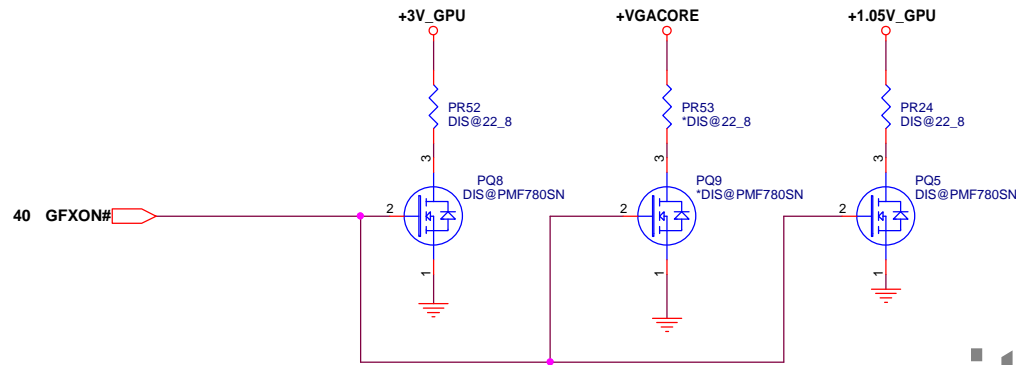


Discrete only

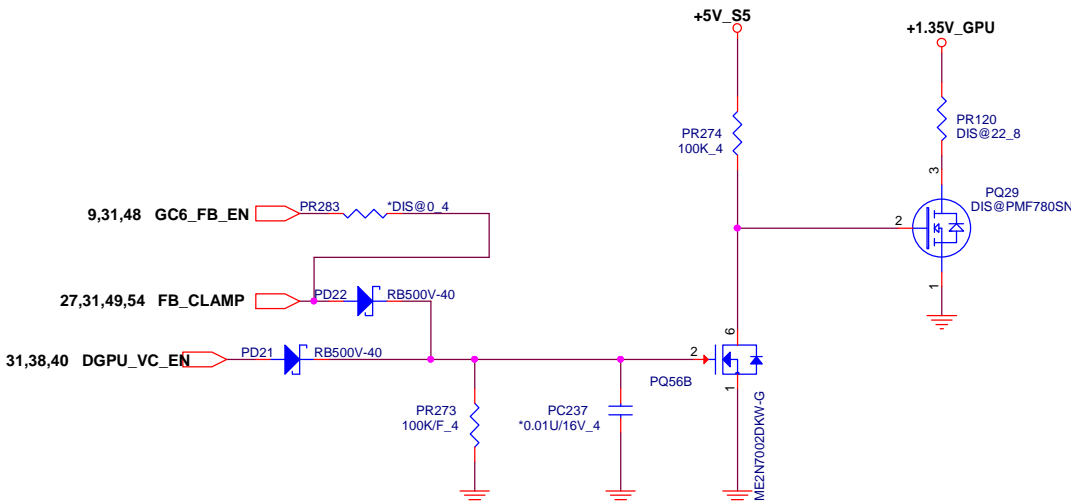
31,40,46,48,49,50 +3V_GPU
38,49,50 +VGACORE
40,46,49,50 +1.05V_GPU
31,46,47,49,50,51,52,53 +1.35V_GPU



50



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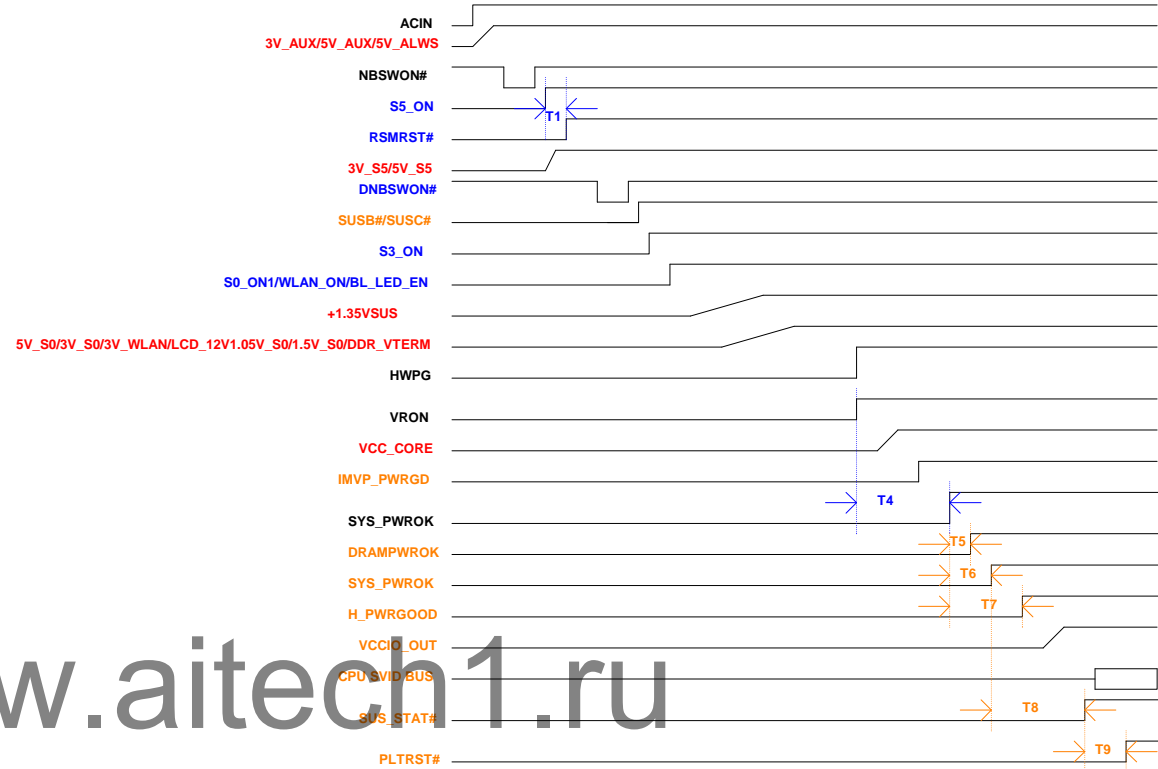
		PROJECT : NL8	
Quanta Computer Inc.			
Size B	Document Number	Rev 1A	
Discrete Discharge			
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POWER Sequence Voltage Rails

Power	Voltage	S0	S3	S4	S5	G3	Ctl Signal
3V_RTC	3V	ON	ON	ON	ON	ON	Adaptor in
VIN	19V	ON	ON	ON	ON	OFF	Adaptor in
5V_AUX	5V	ON	ON	ON	ON	OFF	Adaptor in
3V_AUX	3.3V	ON	ON	ON	ON	OFF	Adaptor in
5V_ALWS	3.3V	ON	ON	ON	ON	OFF	3V_AUX
+3V_S5	3V	ON	ON	OFF	OFF	OFF	S5_ON
12V_S5	12V	ON	ON	OFF	OFF	OFF	S5_ON
+1.35VSUS	1.35V	ON	ON	OFF	OFF	OFF	S3_ON
3V_WLAN	3V	ON	OFF	OFF	OFF	OFF	WLAN_ON
LCD_12V	12V	ON	OFF	OFF	OFF	OFF	BL_LED_EN
5V_S0	5V	ON	OFF	OFF	OFF	OFF	S0_ON
+3V	3V	ON	OFF	OFF	OFF	OFF	S0_ON
+1.5V	1.5V	ON	OFF	OFF	OFF	OFF	S0_ON
+1.05V	1.05V	ON	OFF	OFF	OFF	OFF	S0_ON
+0.65V_DDR_VTT	0.675V	ON	OFF	OFF	OFF	OFF	S0_ON
VCC_CORE	By VID	ON	OFF	OFF	OFF	OFF	VRON

VZ8H SYSTEM POWER-ON SEQUENCE

02



System Power Sequence

EC Control:

T1: S5_ON TO RSMRST# = 20ms (spec:mini 10ms)

T3: S0_ON2 TO VRON = 10ms

T4: HWPG TO MPWROK > 5-99ms

Note:HWPG NEED TO BE HIGH at that time

System:

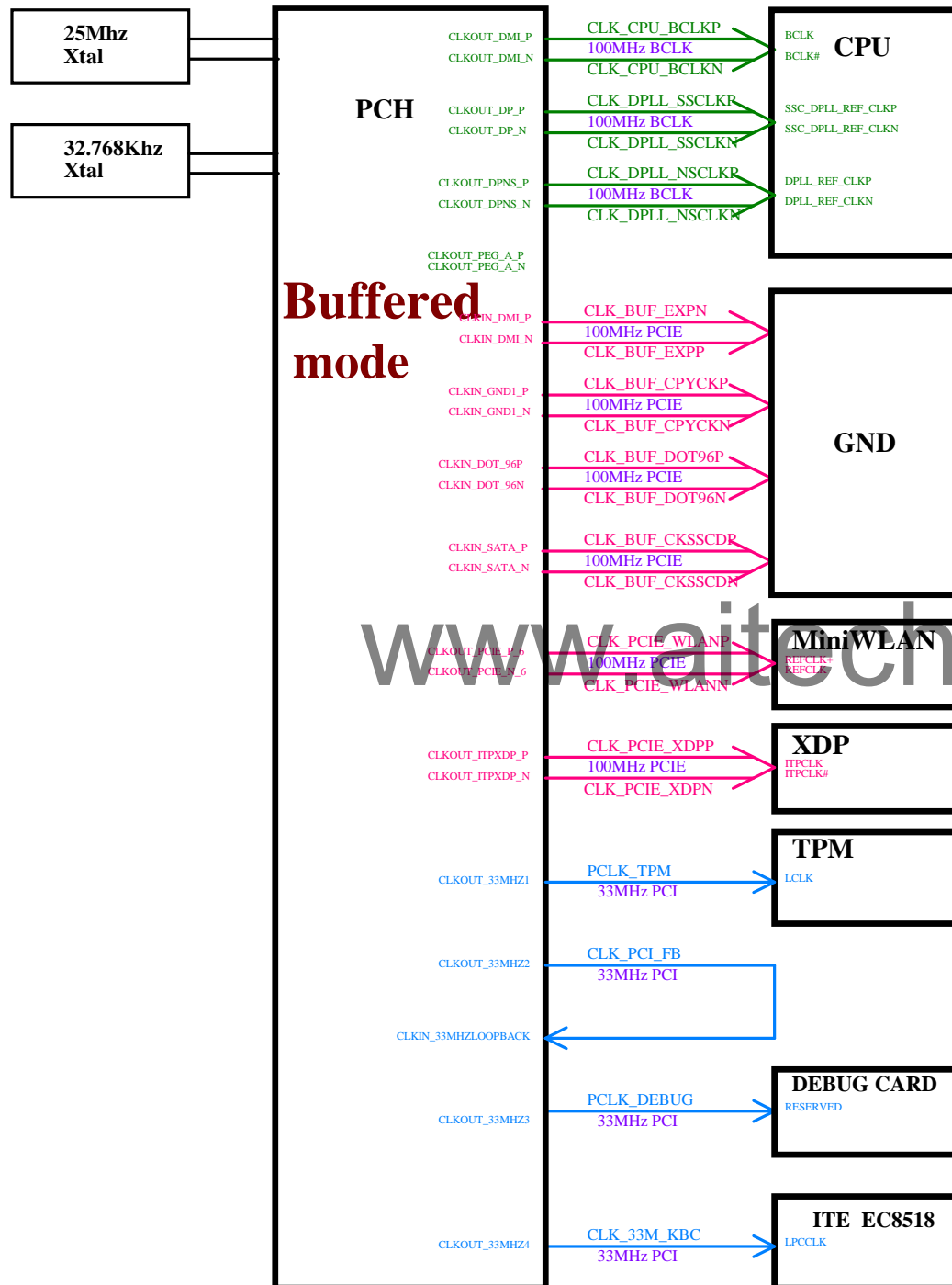
T5: MPWROK to DRAMPWROK > 0us(min)

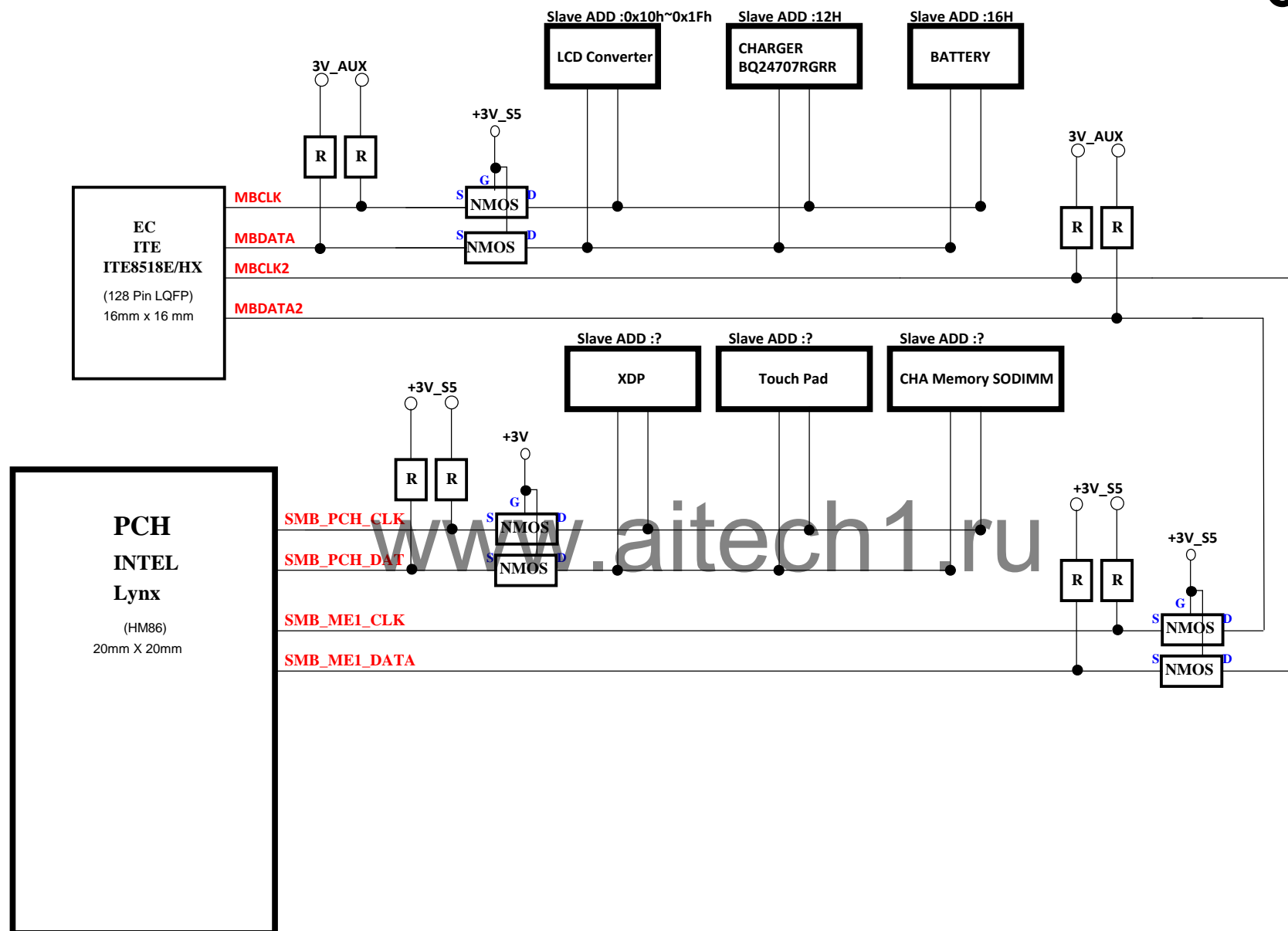
T6: HWPG to SYS_PWROK =5-99ms

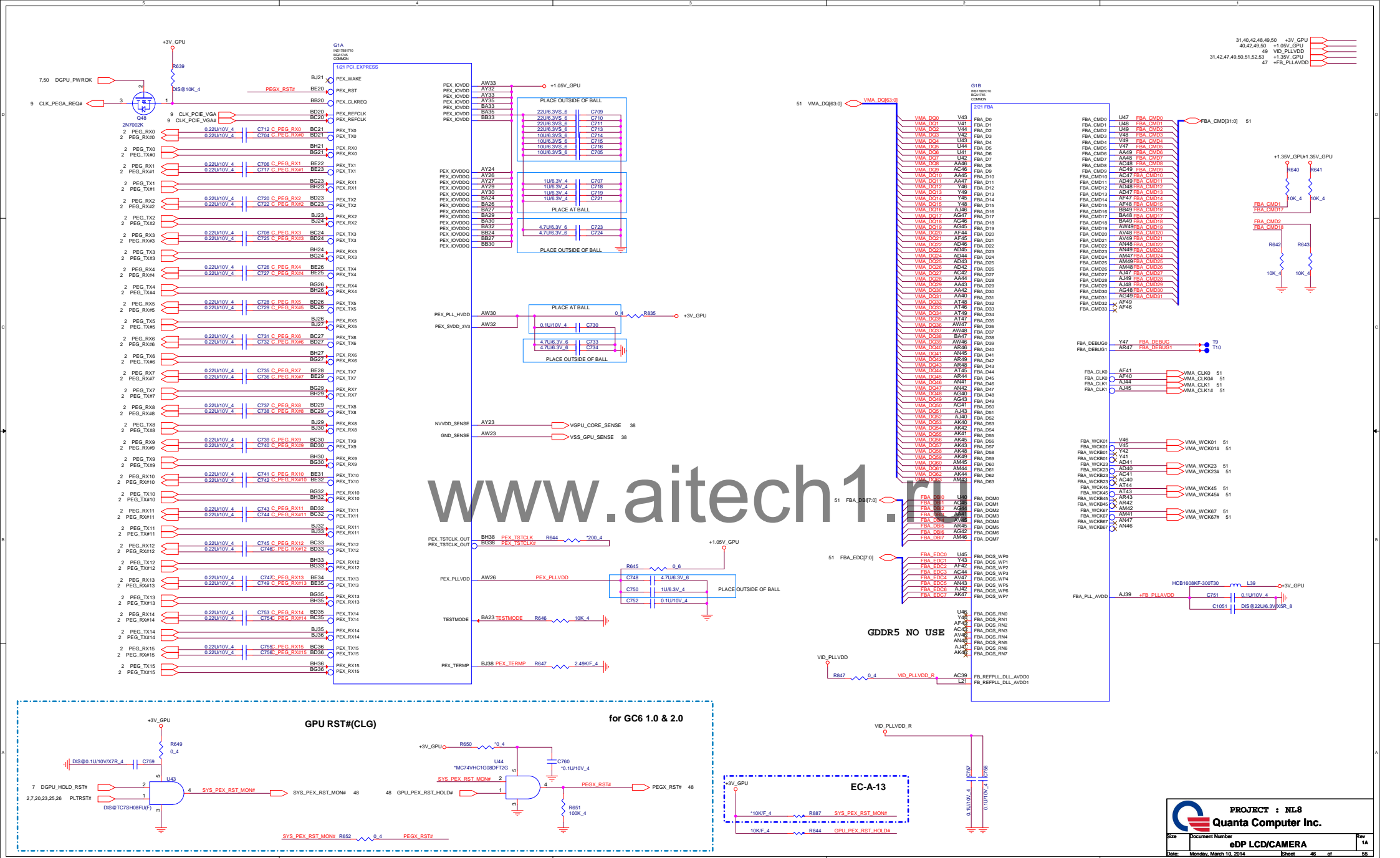
T7: MPWROK to H_PWRGOOD =2ms(Min)

T8: SYS_PWROK to SUS_STAT# =1ms(Min)

T9: SUS_STAT# to PLTRST# =60us(Min)







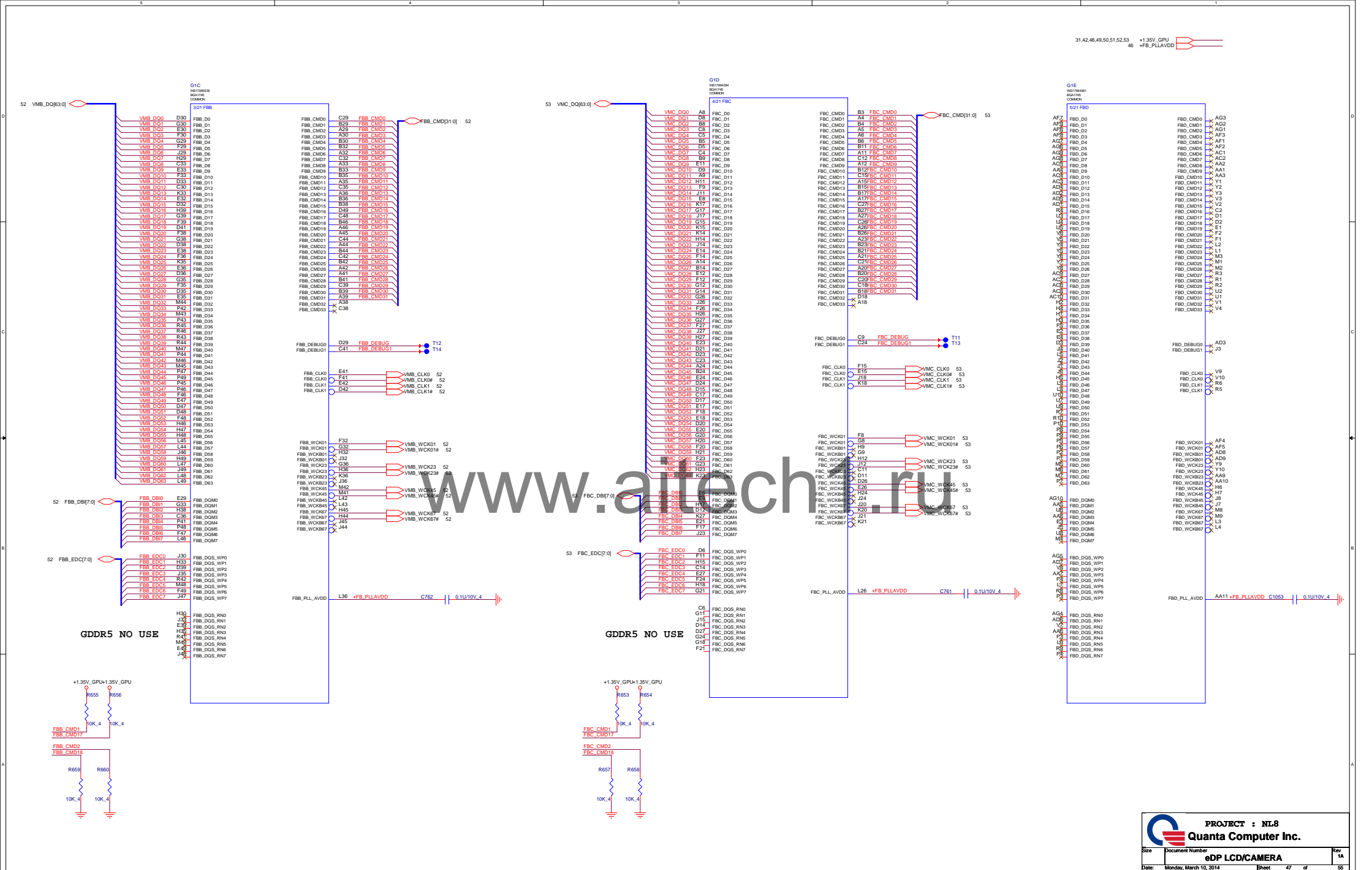
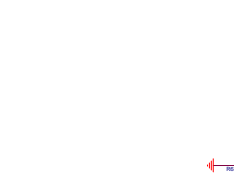
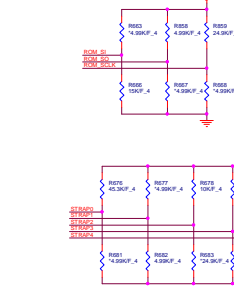


Table 15-2. Resistance Mapping to Hex Values

Resistor Values	Pull-Up to 3V3_MAIN	Pull-Down to GND
4.99 kΩ	1000	0000
10.0 kΩ	1001	0001
15.0 kΩ	1010	0010
20.0 kΩ	1011	0011
24.9 kΩ	1100	0100
30.1 kΩ	1101	0101
34.8 kΩ	1110	0110
45.3 kΩ	1111	0111

Table 15-3 and Table 15-4 contain mapping tables for the Multi-Level Strapping Modes.

NOTE: 1. 0.1mm 0603 1206 SMD. 2. 0.1mm 0603 1206 SMD.



N15E-GX/GT GDDR5 MEMORY RVL

NOTE: 1. N15E-GX/GT, the maximum allowable memory row temperature is 110 °C, as there are no higher end flagchip GPUs.

Memory Type	FB/DDR/ FB/DDR	Memory Density	Manufacturer	Part Number	Die Version	Speed	Memory Speed (x16)	Memory Data Rate (x16)	Status
GDDR5	1.35V/ 1.35V	128MB/16	Samsung	4400032PFC-F103	D-04	D-07	2000	N/A	Production candidate
				4400032PFC-F103	D-04	D-07	2000	N/A	Production candidate
GDDR5	1.35V/ 1.35V	256MB/16	Samsung	4400032PFC-F103	D-04	D-07	2000	N/A	Production candidate
				4400032PFC-F103	D-04	D-07	2000	N/A	Production candidate

256K x16	WS0C4124MFR-T2C	AK05P027006
256K x16	K4G41325FC-BC03	AK05P027500

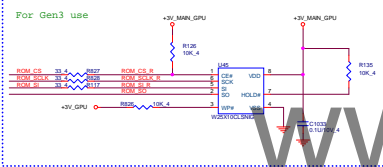


Table 1. N15E-GX / -GT GC6 Pin Assignment

GPIO/ Power Rail	GC6 1.0 Control Signal	GC6 2.0 Control Signal
GPIO1	FB_CLAMP_MON	GC6_FB_EN
GPIO2	FB_CLAMP_TOL_REQ#	GPU_EVENT#
GPIO4	Reserved	3V3_MAIN_EN
GPIO23	Reserved	GPU_PEX_RST_HOLD#
CEC	HC	3V3_PEX_RST_HOLD#
PEX_RST_HOLD	VDD33	3V3_AON
PEX_SYNC_3V3	VDD33	3V3_AON
3V3MISC	VDD33	3V3_AON

Note:
1. All GPIO, GCA/B/C/S, DAC, H/V SYNC, PCM Reset, CLKREQ, XTAL and ATAG signals, when pulled-up, should be connected to the 3V3_AON power rail for GC6 2.0.

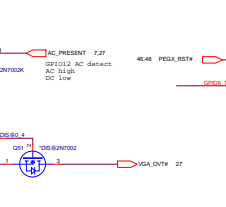
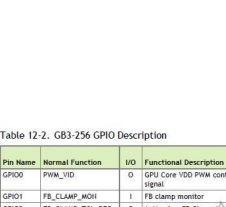
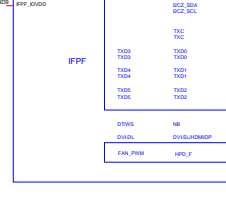
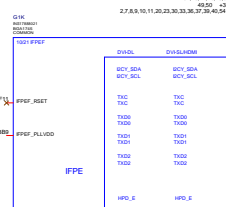
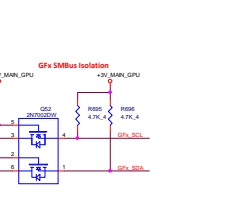
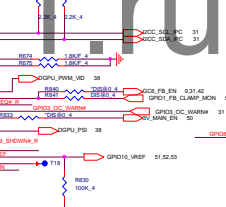
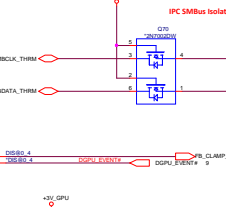
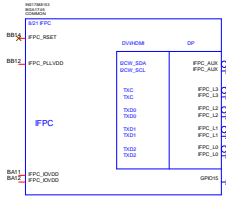
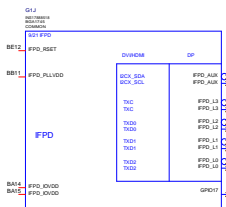
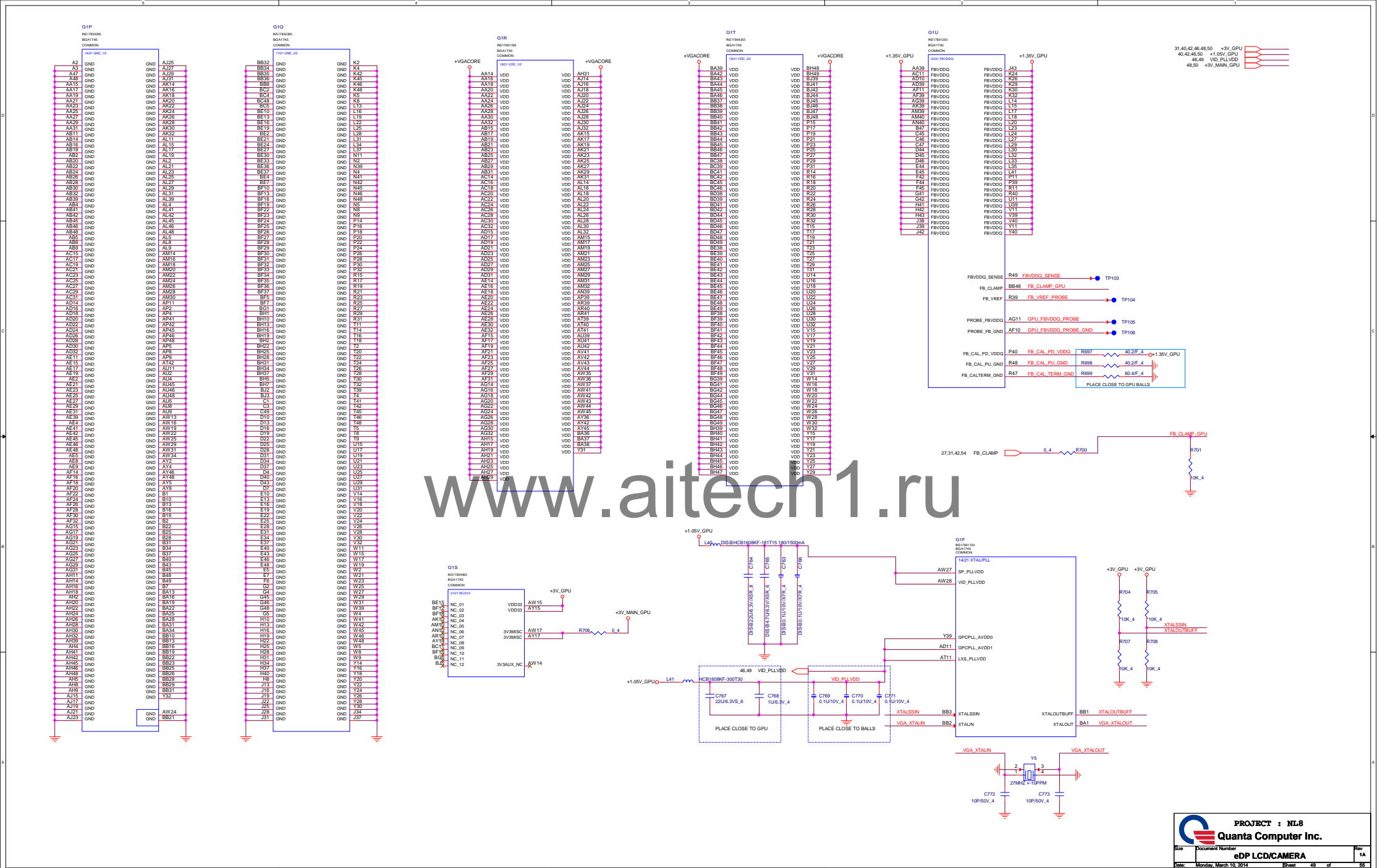
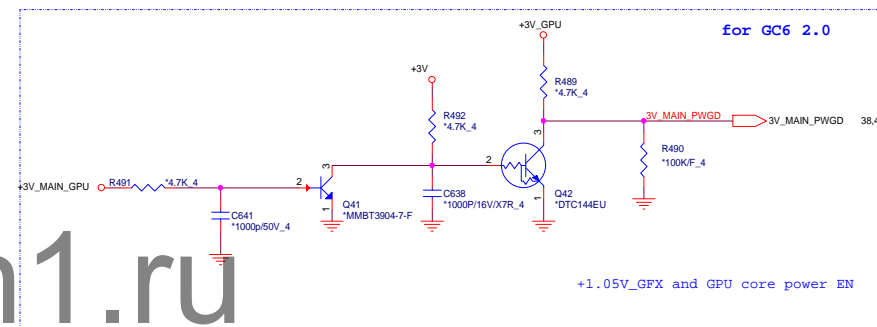
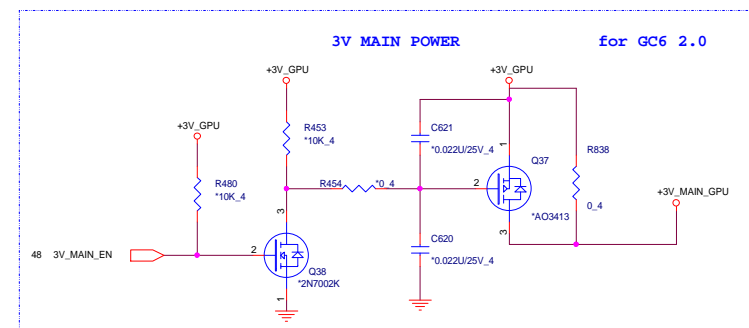
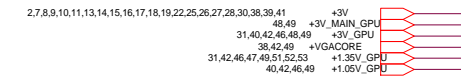
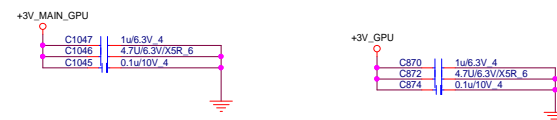
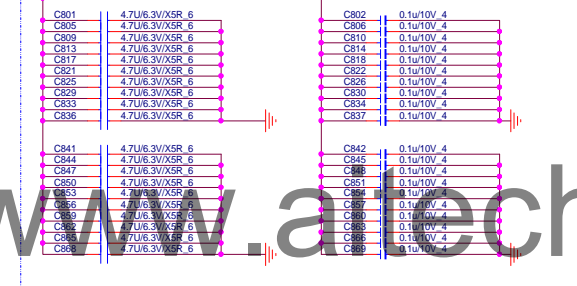
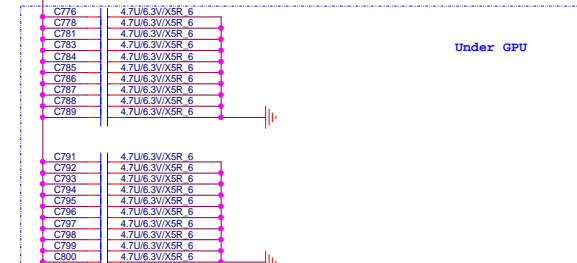
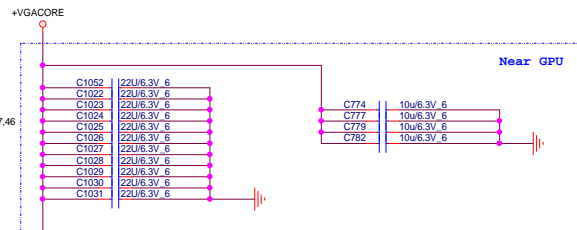
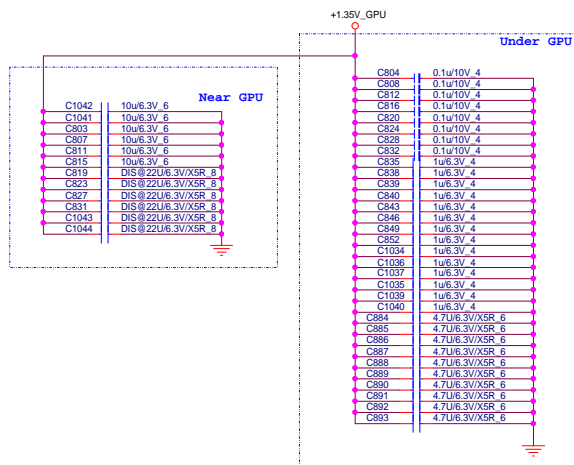
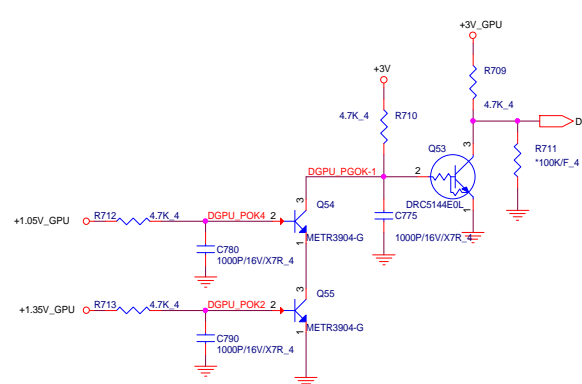


Table 12-2. GB3-256 GPIO Description

Pin Name	Normal Function	I/O	Functional Description	Recommended Default Pull-up or Pull-downs
GPIO0	PWM_VID	O	GPU Core VDD PWM control signal	
GPIO1	FB_CLAMP_MON	I	FB clamp monitor	
GPIO2	FB_CLAMP_TOL_REQ	O	Active low FB Clamp Tolerance request	10K pull-up to system 3.3V
GPIO3	OC_WARN	I	Over current interrupt for IFC	10K pull-up
GPIO4	Reserved			
GPIO6	PSI	O	Phase Shedding	PSI: 10K pull-up to enable two phase.
GPIO7	LCD_PWM	O	Panel Backlight PWM Brightness Control	100K pull-down
GPIO8	QVIRT	O	Active Low Thermal Catastrophic Over Temperature	10K pull-up
GPIO9	ALERT	I/O	Active Low Thermal Alert	10K pull-up
GPIO10	MEM_VREF_CTL	O	Memory VREF Control	100K pull-down
GPIO11	LCD_VCC	O	Panel Power Enable	100K pull-down
GPIO12	PWR_LEVEL	I	AC power detect or power supply overdraw input	100K pull-up
GPIO13	LCD_BLEH	O	Panel Backlight Enable	100K pull-down
GPIO14	HPD_AB	I	Hot Plug Detect for IFPB	See Figure 12-1
GPIO15	HPD_C	I	Hot Plug Detect for IFPC	
GPIO16	HPD_F or HPD_B	I	Hot Plug Detect for IFPF or IFPB	
GPIO17	HPD_D	I	Hot Plug Detect for IFPD	
GPIO18	HPD_E	I	Hot Plug Detect for IFPE	

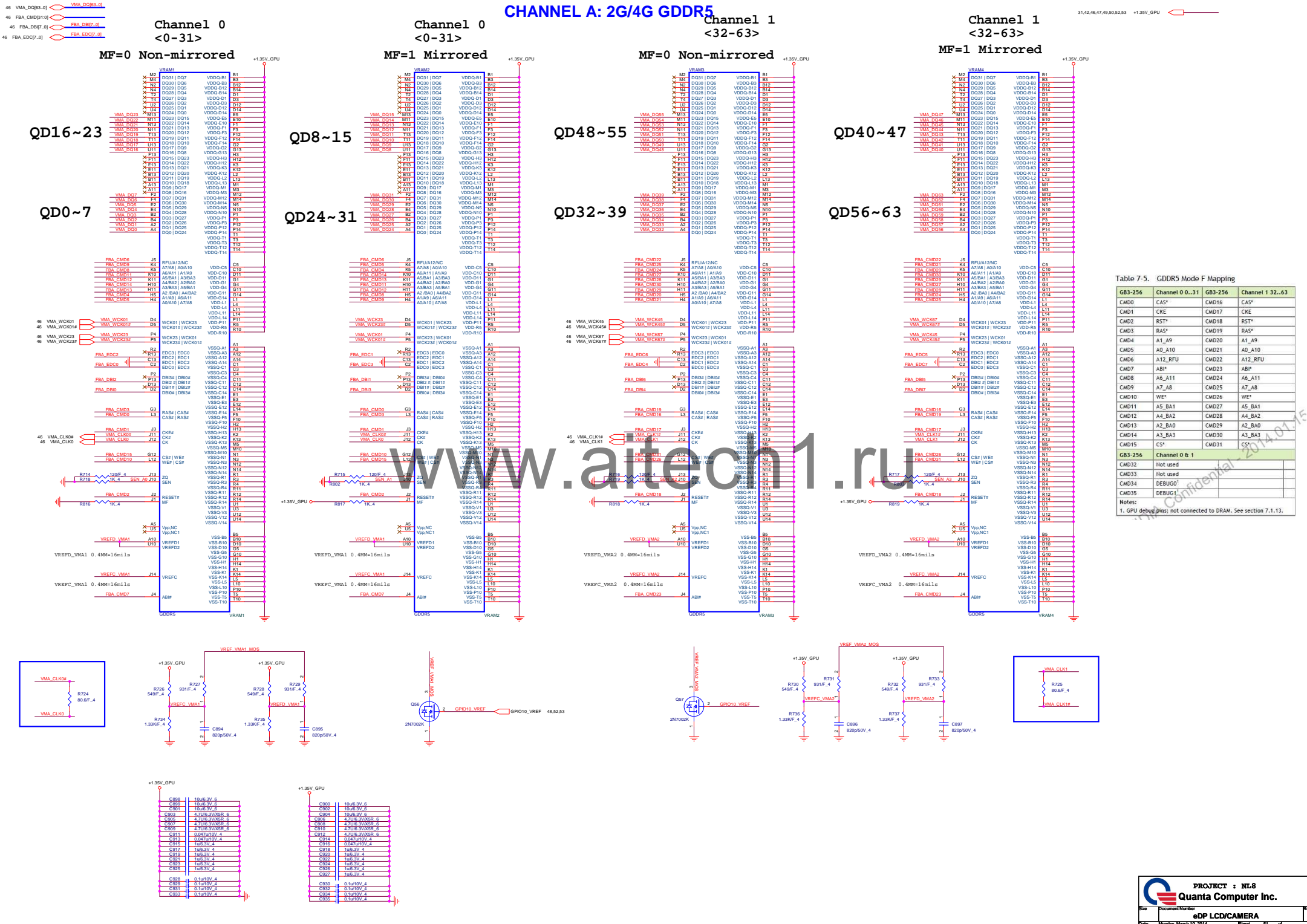




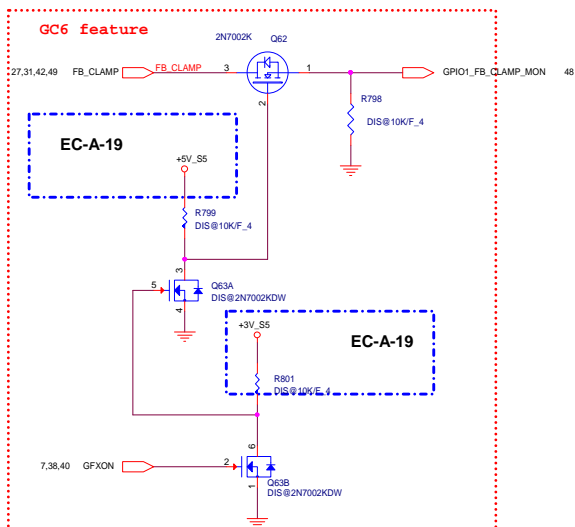
for meet Power down sequence for +3V_GFX



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Power Rail	State in GC6
3V3_AON (New)	On
3V3_MAIN	Off
PEX_1.05V	Off
NVVDD	Off
FBVDD/Q	On

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SDV~SIV

2013

EC NO.	PG.	DATE	PART REFERENCE	DESCRIPTION
EC-A-01	21	02/19	CN20	HDD pin define change.
EC-A-02	26	02/19	Q67	change to Q66A(delete Q67).
EC-A-03	28	02/19	R881,R882,R883	add for current limit
EC-A-04	18,19	02/19	C1058,C1059,C458,R884,C1060	co-lay line and mono-out for subwoofer
EC-A-05	19	02/20	U21	change to AND GATE
EC-A-06	11	02/20	L5	depop
EC-A-07	7	02/20	R862,R863,R536,R548	R862,R863,R536,R548 change to 8.2K
EC-A-08	18	02/20	Q47	Q47 chnage to BAM34090009 for SPDIF LED always tune on issue
EC-A-09	7	02/20	R602	R602 change to 1K to follow CRB
EC-A-10	8	02/20	R526	POP
EC-A-11	48	02/21	R885	reserve 10K for GC6_FB_EN
EC-A-12	48	02/21	R886	reserve R886 for GC6 2.0 GPU_EVENT need pull up to 3V3_AON
EC-A-13	46	02/21	R887	reserve R887 for GC6 2.0 SYS_PEX_RST_MON# need pull up to 3V3_AON
EC-A-14	7,27	02/24	R880	change R880 to 100K pull low and GFXON change from EC to PCH(for GC6 2.0)
EC-A-15	48	02/26	R888,R889	reserve to follow DG but CRB pull low
EC-A-16	28	02/27	R874	change net form KB_LIGHT to KB_LIGHT_P due to same net name as EC control
EC-A-17	24,25	02/27		change U3B(real side) form MB to FB
EC-A-18	9	02/27	R598	add CLKREQ# for card reader and R598 change to pull up
EC-A-19	54	02/27		change power rail
EC-A-20	28	03/04		move LID function to PWR/B
EC-A-21				



PROJECT : ST6A
Quanta Computer Inc.

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	EC list-1	
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